WISCONSIN FORMULA SAE Racing

120kW Quad Inverter for All-Wheel Drive Electric Racecar

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Overview

Due to the lack of off-the-shelf motor controllers that satisfy our power, voltage, safety, and packaging requirements, in-house power electronics were developed for the WR-218e. The quad voltage source inverter (VSI) receives four torque commands from an Electronic Control Unit (ECU) and modulates three-phase current waveforms using a Space Vector Modulation based Field Oriented Control scheme to drive the four permanent magnet motors. The main design goals were as follows: (1) 30kW or 150A_{RMS} continuous per inverter up to 252V, (2) hardware overcurrent, undervoltage, overvoltage, and fault protection that will open IGBT switches in less than 10µs, (3) isolation between the grounded low voltage (GLV) and tractive system, and (4) CAN bus communication.

Design Features

- ✓ 120kW total - 30kW per motor
- ✓ Up to 300V and 280A phase current
- ✓ Switching frequency: 20kHz
- ✓ Self-sensing Field Oriented Control and Space Vector Modulation PWM
- ✓ CAN interface
- ✓ Hardware overcurrent and overvoltage protection that reacts in less than 10µs
- ✓ Isolated HV and LV systems
- ✓ Reverse voltage, undervoltage, overvoltage protection of LV system
- ✓ IGBT junction, DC link capacitor, and motor winding temperature sensing
- ✓ CFD optimized cold plate
- ✓ Waterproof enclosure

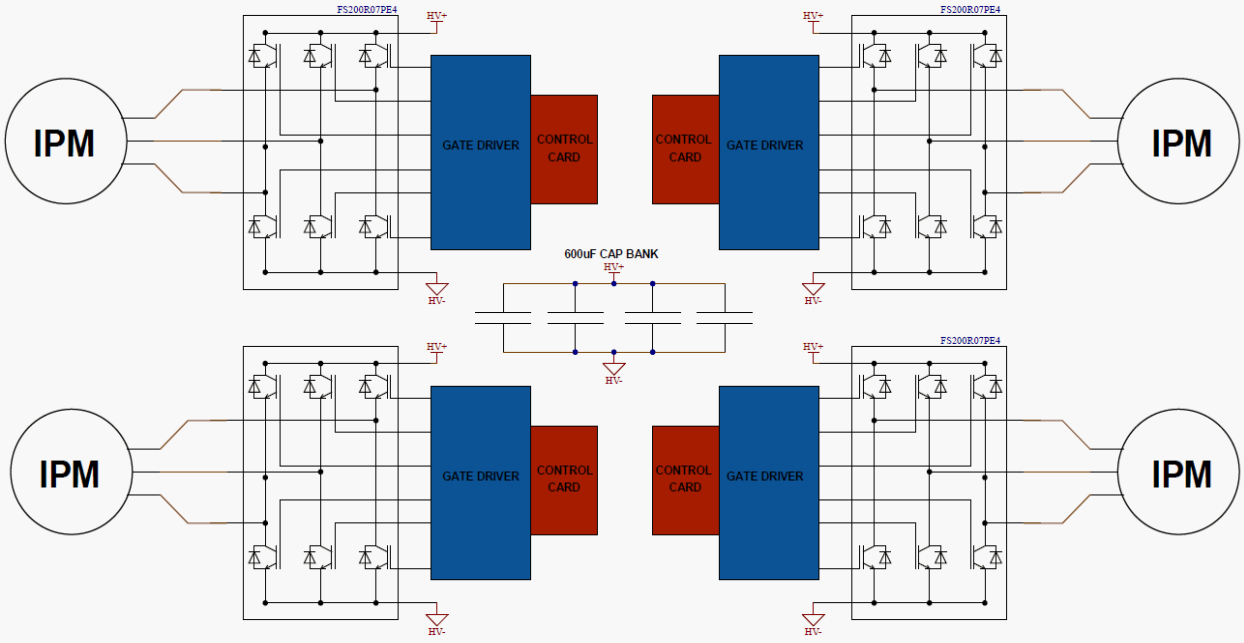

Figure 1: Simplified Representation of Quad Inverter

Table of Contents

Acronyms

AC – Alternating Current

ADC – Analog-to-digital converter

BJT – Bipolar junction transistor

BMS – Battery Management System

CAN – Controller Area Network

CMC – Common Mode Choke

CFD – Computational Fluid Dynamics

CMTI - Common-Mode Transient Immunity

CPU – Central processing unit

DC – Direct Current

DVP&R – Design Validation Plan and Report

DSP – Digital Signal Processor

ECU – Electronic Control Unit

EMI – Electromagnetic interference

EMF – electromotive force

ESR – Equivalent Series Resistance

ESL – Equivalent Series Inductance

GaN – Gallium Nitride

GLV – grounded low voltage

GPIO – General Purpose Input Output

HRPWM – High Resolution Pulse Width Modulation

HV – High Voltage

I/O – Input/Output

IC – Integrated Circuit

IGBT – Insualted Gate Bipolar Transistor

IPM – Interior Permanent Magnet

JTAG – Joint Test Action Group

MCU – Microcontroller Unit

MOSFET – Metal-Oxide-Semiconductor Field-Effect Transistor

NTC – Negative Temperature Coefficient

OTS – Off the shelf

PCB – Printed Circuit Board

PPR – Pulse Per Revolution

PSSR – Power Supply Rejection Ratio

PWM – Pulse Width Modulation

RC – Resistor-Capacitor

RGB – Red-green-blue

RL – Resistor-Inductor

ROM – read-only memory

SiC – Silicon Carbide

TI – Texas Instruments

UART - Universal Asynchronous Receiver-Transmitter

VIN – Voltage In

WBG – wide bandgap

WEMPEC – Wisconsin Electric Machines and Power Electronics Consortium

Motivation – Why did you decide to make your own inverter?

1. Nothing off-the-shelf (OTS) satisfied our requirements
2. Learning
3. Opportunity to do something that no one else has done before

The main driving factor behind why we journeyed into the mysterious land of power electronics was because we looked at all the motor controllers available on the market and none of them satisfied our requirements.

- DC voltage – Can the inverter operate at a DC bus voltage of 100V-300V? Anything less 100V(ish) and you have a very large amount of DC link current needed to reach 80kW and anything more than 300V will violate the 2017-2018 Formula SAE rules [1].
- Galvanic isolation – Are the high voltage (HV) and low voltage (LV) systems galvanically isolated?
- AC Power – How much power can it supply to a motor? What's the maximum phase current it can handle?
- Motor fundamental frequency – Can the inverter switch fast enough to safely control a motor with a relatively high fundamental frequency?
- Hardware protection – Will the inverter explode in the case of an overcurrent or overvoltage fault? Or will it protect itself?
- Packaging requirements – Is the inverter small enough where it can package without interfering with the battery, frame, and firewall?
- CAN/Power interface – Can it interface with the car's GLV system without any additional modifications?
- Robustness – Can it handle a motorsports environment in terms of the acceleration/vibration that it will see? Is it waterproof?
- Weight – Does it weigh 50 pounds? This is motorsports. Every gram matters.

We asked these questions when looking at OTS inverters and were not able to find a solution that met our requirements. Again, this was the primary reason behind developing our own motor controller, but also was a great way for us to experientially learn about power electronics and do something unprecedented. We were the first United States team to do all-wheel drive in 2017 so we felt compelled to keep pushing forward with innovation.

Architecture

The first step in designing anything is defining your requirements. It is extremely important that these are comprehensive and defined clearly. There's no justification for designing something anything better than what the requirements dictate. One set of requirements is defined by whatever the device interfaces with. Really think these through! This is the prime location for screwing up. Systems integration is almost always the toughest part of any project. In the case of the quad inverter, it interfaces with the battery pack, four permanent magnet motors, vehicle low voltage system, cooling system, and the frame. The next set of requirements is defined by the resources you have available - time, expertise, equipment, sponsors, etc. Capabilities ultimately drive project requirements. For example, our technical capabilities heavily influenced our processor selection and our decision to use InstaSPIN. We'll get to this in a minute. Below is the list of requirements that we initially defined for the inverter.

Requirements

- Individual control of four motors
    - Bus voltage: 180V – 252V
    - Peak power ≈ 30 kW mechanical, 33kW electrical
    - Peak torque ≈ 30Nm
    - Base speed ≈ 9500RPM
    - Top speed ≈ 20000 RPM
    - # of poles = 10
    - Switching frequency = 20 kHz
    - Fundamental frequency = 1.67 kHz
    - D-axis inductance ≈ 90 μH
- Torque control
    - Field Oriented Control
        - Maximum torque per ampere
        - Field weakening
    - Space Vector Modulation PWM
- InstaSPIN requirements
    - Processor must be one of the following:, F28068F, F28062F
    - 3 phase current feedback signals
    - 3 phase voltage feedback signals
    - Bus voltage feedback signal
- Protection
    - IGBT (open gates in <10μs)
        - Desaturation detection (shoot-through protection)
        - Phase-phase overcurrent

        - DC bus overvoltage/undervoltage protection
        - Gate clamping
        - IGBT die overtemperature
    - Processor watchdog
    - Voltage supervision on voltage supply rails for logic and gate drive
    - Overvoltage, undervoltage, and reverse voltage on low voltage input
    - Failure propagation prevention
    - 3mm isolation zones
    - Conformal coating to reduce creepage constraints
- Physical packaging requirements
    - Two DC cables in, 12 phase out
    - < 10kG
    - Waterproof
    - Liquid cooling
- 350A DC continuous in high current path
- Isolated CAN input – 1 Mbps
- Low voltage supply: 12V – 15V
- Status indicators for each inverter

Once these high-level requirements were defined, we selected the main components of the system and started brainstorming how the components would be laid out in the housing.

InstaSPIN

We decided to use InstaSPIN-FOC™ with Texas Instrument's CONTROLSUITE libraries to help speed up development time for implementing SVM Field Oriented Control with max torque-per-ampere and flux weakening control. InstaSPIN has a host of useful features that you can read about in their User Guide [2], but the most notable are:

- Accurate angle estimation at steady state speeds below 1 Hz with full torque
- Motor parameter identification
- Automatic torque (current) loop tuning, with option for user adjustments
- DC bus voltage compensation
- Automatic offset calibration
- High quality flux and rotor flux estim[3ation

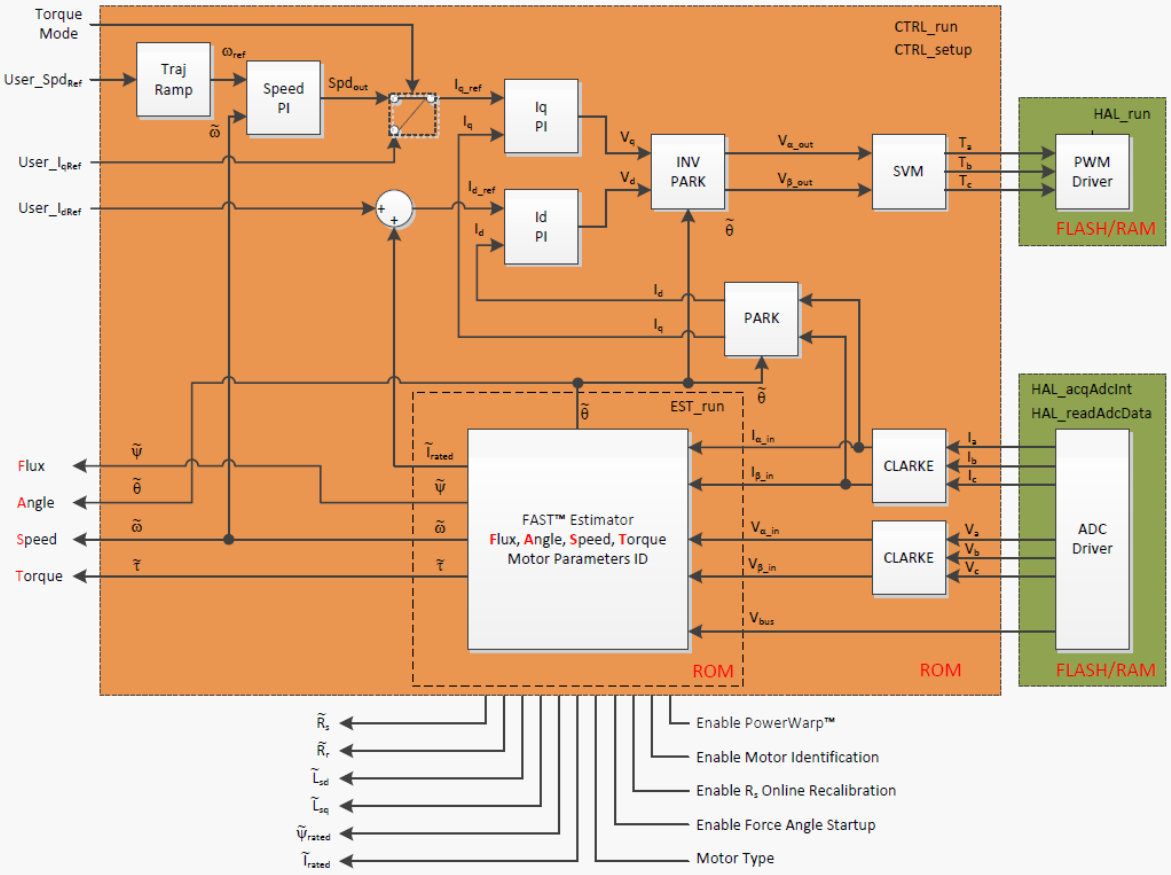

Figure 2: InstaSPIN Block Diagram

InstaSPIN-FOC™ allowed us to implement sensorless control without too much trouble. Its FAST estimator algorithm uses phase current, phase voltage, and DC bus voltage for Flux, Angle, Speed, and Torque estimation. These feedback signals dictated which sensors were needed for motor control.

- Three phase voltages
- Three phase currents
- DC bus voltage

Self-sensing of rotor position meant that no encoder or resolver was needed on the motors. This simplified the system tremendously as it eliminated the need for a resolver-to-digital converter, isolated power supply, and the connectors needed to interface with the sensor. Complexity is defined by the number of interfaces in the system. More often than not, the least complex system is the most reliable. Thus, our goal was to minimize the number of interfaces and design the simplest system possible while still satisfying requirements. Self-sensing is a great example of one way we did that.

Processor Selection

The decision to use InstaSPIN dictated which processor we had to select. As shown in the table below, TI sells a host of processors specifically designed for the InstaSPIN platforms. These processors have special libraries loaded in the ROM that allow InstaSPIN to work its magic.

	InstaSPIN Solution	MHz	FPU	CLA Co-Processor	Motors	Flash (KB)	12b ADC Chs	PGA	CAN	QEP	USB	SPI	UART	I2C	Pins	Temp
F28069M	-MOTION	90	Y	Y	1 or 2	256	16 or 12	--	1	1	1	2	2	1	100/80	-40 to 105° C
F28068M	-MOTION			--		256										
F28069F	-FOC			Y		256										
F28068F	-FOC			--		256										
F28062F	-FOC			--		128										
F28054M	-MOTION	60	--	--	1 or 2	128	16	4	1	1	--	1	3	1	80	-40 to 125° C Q100
F28054F	-FOC					128										
F28052M	-MOTION					64										
F28052F	-FOC					64										
F28027F	-FOC	60	--	--	1	64	13	--	--	--	--	1	1	1	48	
F28026F	-FOC					32										

Figure 3: InstaSPIN Processor Matrix

The F28069F was the obvious choice as it satisfied our requirements and was the fastest processor available.

TMS320F28069F Specs [3]

- 90 MHz 32-Bit CPU
- Floating-Point Unit
- Programmable Control Law Accelerator
    - 32-Bit Floating-Point Math Accelerator
    - Executes Code Independently of the Main CPU
- 256KB of Flash and 100KB of RAM
- Single 3.3-V Supply and No Power Sequencing Requirement
- Watchdog Timer Module
- Peripherals
    - 8 Enhanced Pulse-Width Modulator Modules
    - 12-Bit Analog-to-Digital Converter (ADC), Dual Sample-and-Hold
    - Two Serial Communications Interface [UART] Modules
    - One Enhanced Controller Area Network
    - 54 Individually Programmable GPIO

Semiconductor Switch Selection

The requirements of the semiconductor switches were largely a function of the motor design. For example, to achieve the target torque of 30Nm, we needed 170A of phase current. Based on the targeted motor specs, we identified the following requirements for the semiconductor switches.

- Collector-emitter blocking voltage > 600V
- Collector current > 170A nominal
- Temperature sensing of the silicon die
- Busbar connections for phase and DC bus – sixpack module preferred
- Electrically isolated thermal baseplate
- >90% efficiency when switching at 20kHz
- Operation up to 100°C

SiC and GaN were initially considered due to their advantageous properties over IGBTs. Wide bandgap devices are superior over IGBTs in terms of dielectric strength, high-speed switching, tolerance of high operating temperature environments, high current density and low on-resistance. With that said, there are currently no SiC/GaN sixpack modules offered that satisfy our collector/drain current requirements. We did not want to use discrete components as this would significantly increase design complexity for the cold plate thermal interface. Additionally, we wanted to keep all high current off the PCB since this would require specialized manufacturing services to achieve the trace thickness required. We did not have these services available to us, so busbar connections were preferred.

The most compact solution that satisfied all our requirements was the FS200R07PE4 [4] from Infineon. This is a sixpack module so there are six IGBT switches arranged in a two level, three phase configuration.

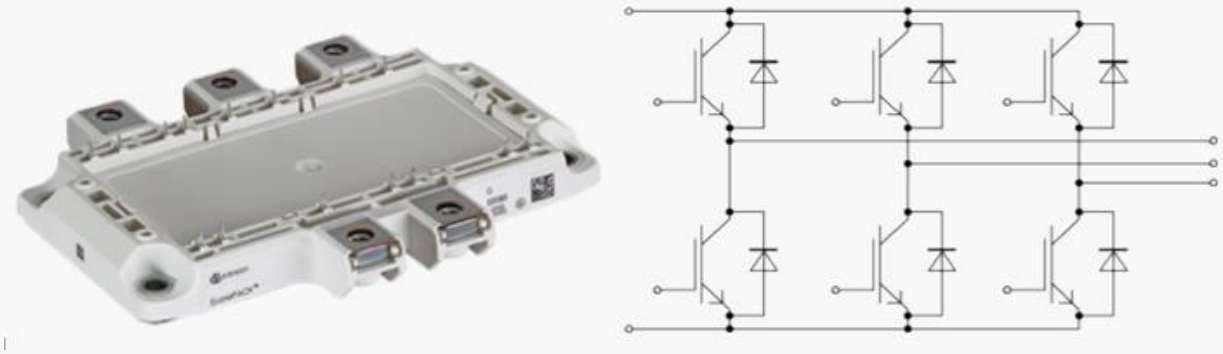

Figure 4: FS200R07PE4 Infineon sixpack IGBT module

Collector-Emitter Voltage	650V
Continuous DC Collector Current	200A

Temperature	-40°C – 150°C
Size	130mm x 100mm
Weight	400g

The thermal interface on the FS200R07PE4 is very straightforward. There is an electrically isolated baseplate that a cold plate can be easily mounted to using the four M5 holes provided. The module has an NTC thermistor that can be used to read the temperature of the IGBT die. Finally, there is a kelvin connection on the emitter of each IGBT switch to reduce inductance in the gate-emitter loop.

Before proceeding forward, we did some thermals simulation using Infineon's IPOSIM tool [5] to get an idea of how much heat we'd have to reject based on the phase current. The simulation takes into account both switching and conduction losses.

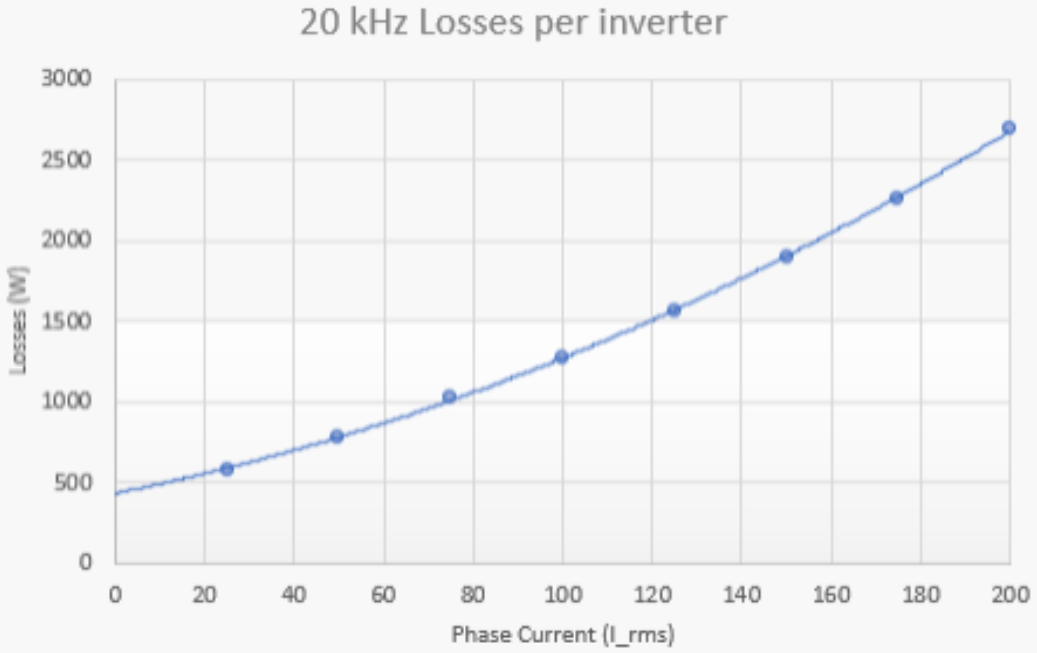

Figure 5: Power losses (Watts) vs. Phase Current (A_{RMS}) at 20kHz switching frequency

The results were reasonable, so we decided to move forward with using the FS200R07PE4.

DC Link Capacitor Selection

In a voltage source inverter, the DC link capacitor has two main responsibilities -

1. Supply AC part of IGBT module current - Battery pack cannot source current at the fundamental frequency + harmonics due to inductance of cables and battery busbars.

2. Stiffen the DC bus - Decouple the effects of stray inductance from the DC voltage source to the power bridge.

With traction inverters, the ripple current is typically the driving factor that dictates which capacitor is selected. This is primarily why almost all modern traction inverters use film capacitors. They have a low equivalent series resistance (ESR) and equivalent series inductance (ESL) so they have a high ripple current rating. You can get all the capacitance you want with electrolytic capacitors, but the ESR and ESL are much higher compared to film capacitors so you need to put many of them in parallel in order to satisfy the ripple current requirement [6]. The volumetric efficiency ends up being much higher if film capacitors are used. In addition, InstaSPIN includes DC bus voltage ripple compensation so the ripple voltage requirement was very loose because of that.

DC Link Capacitor Ripple Current Rating

When a DC voltage is converted to a train of variable-width pulses using power semiconductors, the switched output voltage contains a rich spectrum of high-order switching harmonics in addition to the target fundamental. The second consequence is that smooth AC output currents are fed back into the DC link as a train of current pulses so the overall DC bus is the superposition summation of the switched current pulses from each phase leg. You end up with a complex harmonic spectrum that is very difficult to analytically solve for [7]. Thus, we used simulation to determine the ripple current requirement. We modeled the battery as a voltage source in series with an inductor and resistor. The cables were modeled as an RL circuit and the capacitor was modeled as a RC circuit.

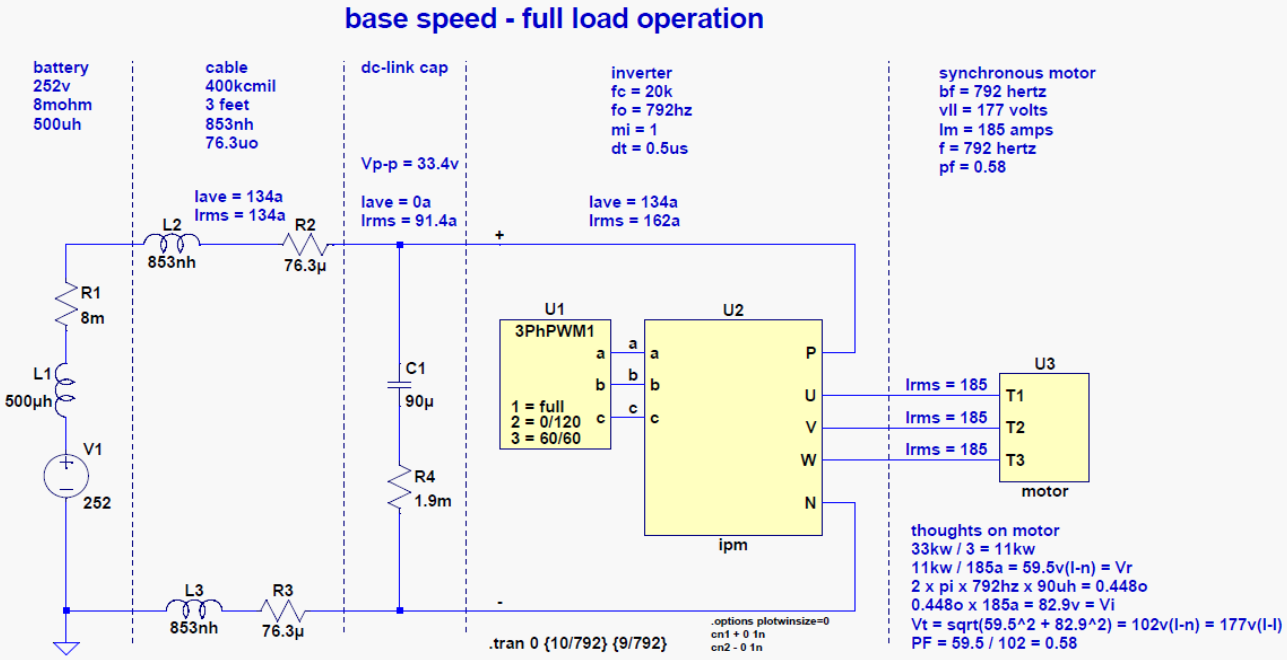

Figure 6: Simulation schematic used for sizing DC link capacitor bank

The graph below shows the capacitor current over a few cycles. This assumes the capacitor is supplying the AC part of the IGBT module current and the battery is supplying the DC current.

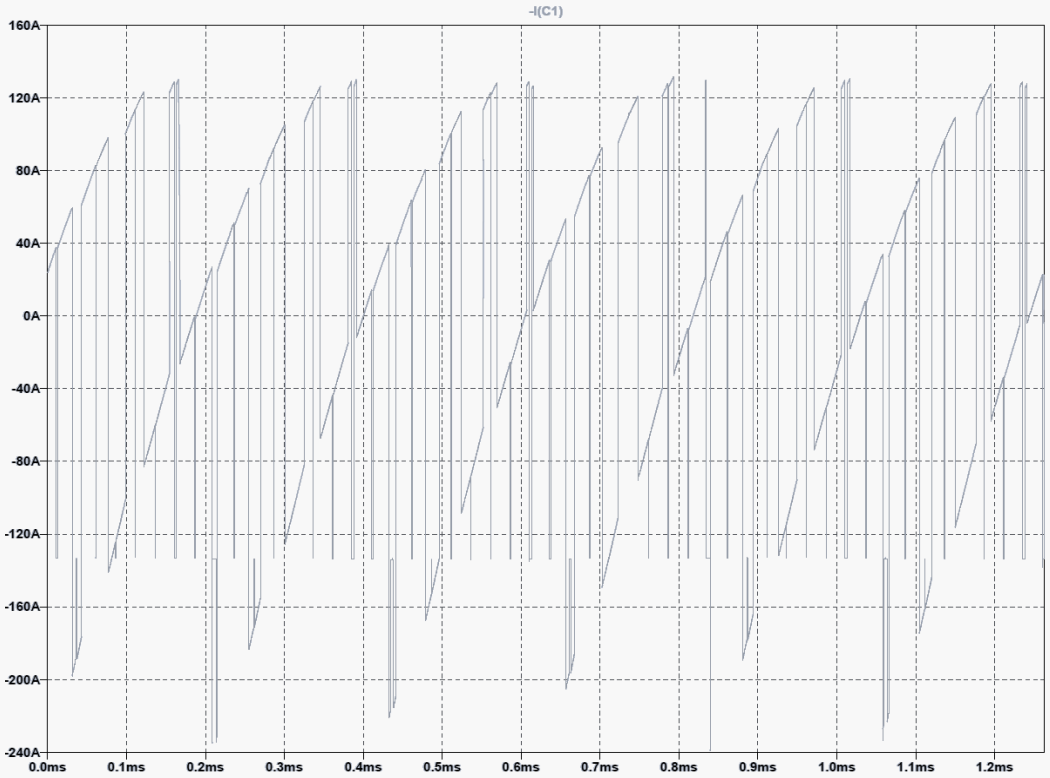

Figure 7: Capacitor current over several duty cycles

Simulations were run for full load at varying duty cycles. The results are summarized in the table below showing current splits and voltage ripple for duty cycles of 25%, 50%, 75%, and 100%.

f(output)	duty cycle	I(battery)	I(cap)	I(module)	V(cap)	V(ripple)
792hz	100%	134A_{DC}	91.4A_{RMS}	164A_{RMS}	33.4V_{p-p}	13.2%
594hz	75%	99.2A_{DC}	97.8A_{RMS}	139A_{RMS}	25.4V_{p-p}	10.1%
396hz	50%	66.4A_{DC}	92.9A_{RMS}	114A_{RMS}	18.8V_{p-p}	7.5%
198hz	25%	33.5A_{DC}	74.3A_{RMS}	81.5A_{RMS}	14.3V_{p-p}	5.7%

As you can see, the worst-case capacitor current occurs right around 75% duty cycle. If our assumptions were correct, we could see as much as 98A_{RMS} in the DC link capacitor(s).

DC Link Capacitor Voltage Rating

The voltage rating of the DC link capacitor was determined by the flux weakening fault scenario. When an IPM motor is operating in its flux weakening region and a fault occurs, a large voltage can develop

on the motor terminals [8]. We calculated this voltage to be approximately 550V based on the law of conservation of energy – $3*1/2*L_{l\text{-}n}*I^2$ into the $1/2*C*V^2$ of the caps + the natural back EMF at that speed. Film capacitors can withstand a DC potential of 1.3x rated voltage for one minute without damage or breakdown so we selected a capacitor with a nominal voltage rating of 500V.

With the voltage rating and ripple current rating defined, we selected the shortest capacitor that satisfied those requirements. We decided to use the UL3 Q157K from Electronics Concepts [9]. These are polypropylene film capacitors with a low profile of just 40mm and excellent ESR and ESL ratings of 0.47mohms and 12nH.

Current Sensor Selection

The following requirements were defined for current sensing.

Nominal Current	150A
Max Current	300A
Accuracy	1%
Bandwidth	>40kHz
Supply Voltage	3.3V – 5V
Output Voltage	0 – 3.3V

There were three technologies that were considered; hall effect, shunt, and fluxgate sensors. The current shunt solution is likely the smallest and lightest, but you must deal with considerable common mode voltages, temperature drift, and then conditioning/isolating the signal. Accuracy and bandwidth are compromised in the conditioning and isolation stages of the signal chain. Flux-gate sensors are a rather new technology that offers high accuracy across a large current range. However, these sensors need to be centered in a slot, cut out in the middle of a busbar. It is very simple and straightforward to just have the phase cable connect directly to the IGBT phase terminal and then have a hall effect sensor around the cable. We decided to go with the HO 150-S/SP33-1106 hall effect current sensor [10] as it was the simplest solution that satisfied all the requirements listed above.

Figure 8: LEM HO 150-S/SP33-1106 Open Loop Hall Effect Current Sensor

Quad Inverter Layout

Once we selected the main components, we started thinking about what the most space-efficient layout would be to package the IGBTs, capacitors, current sensors, cold plates, and the PCBs. We went through a few different iterations and arrived at the configuration shown below. This resulted in the least amount of unutilized space and offered the highest power density.

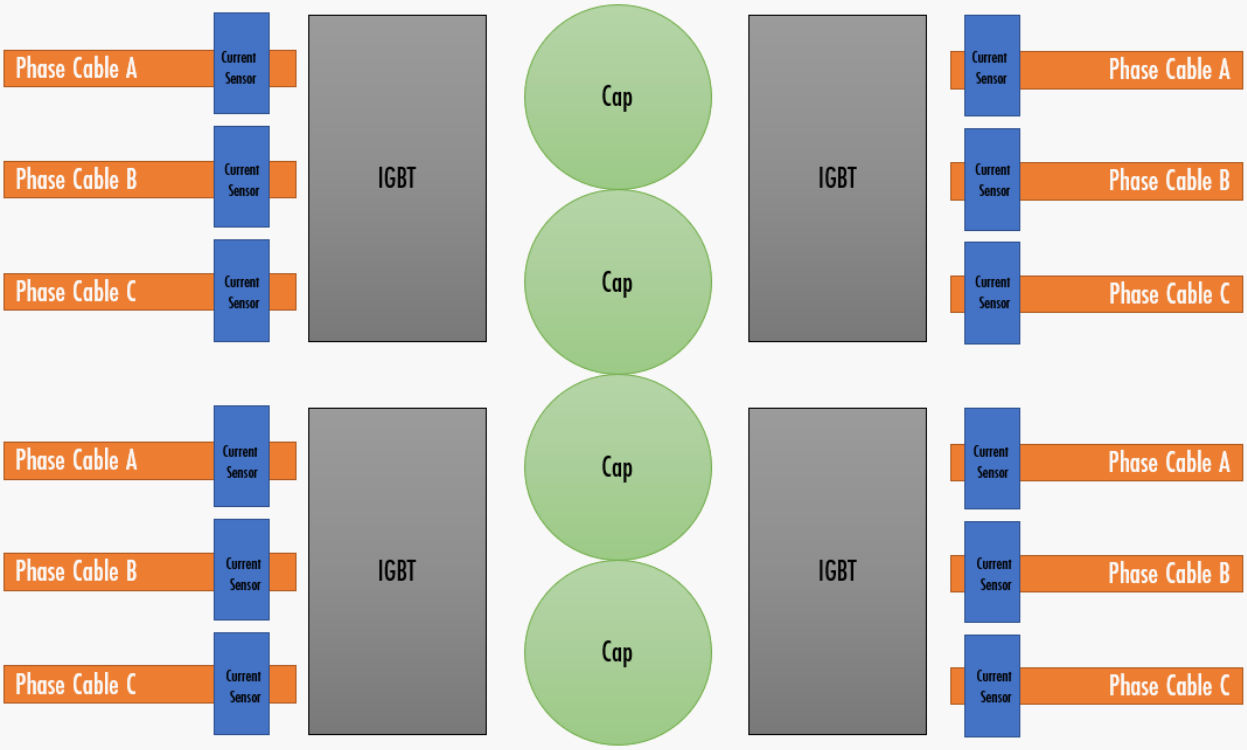

Figure 9: Quad Inverter Layout

Schematic Design

Each individual inverter is broken up into three separate boards to improve modularity and maximize packaging density. This is shown in the graphic below.

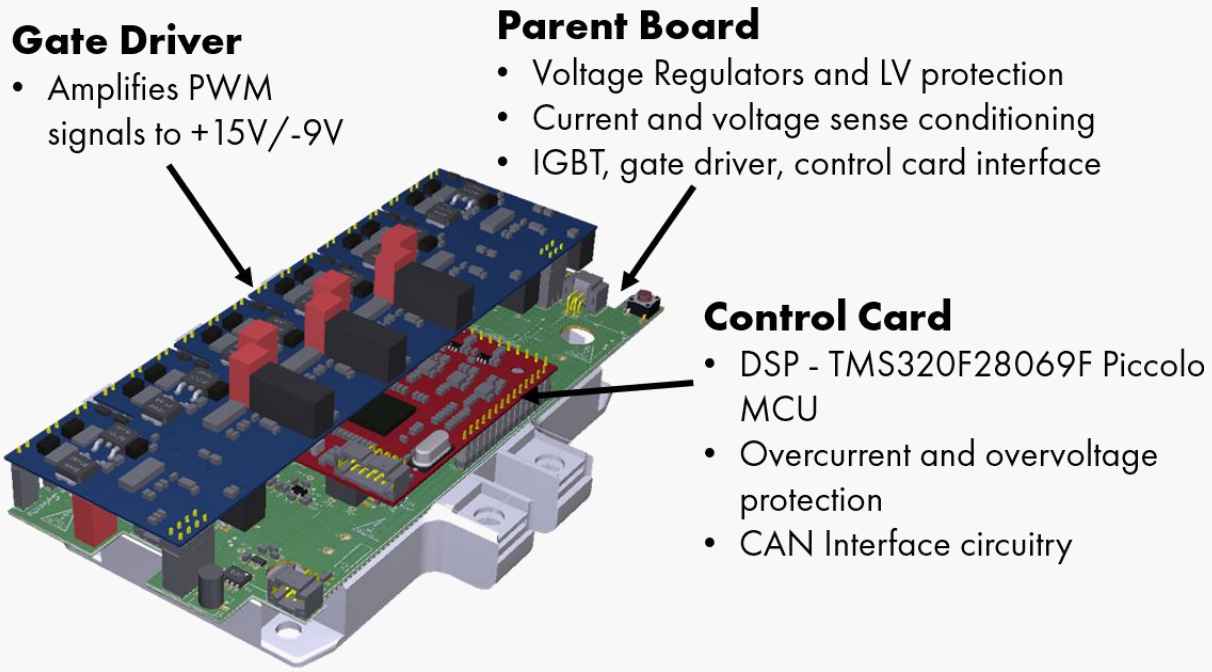

Figure 10: PCB assembly for a single inverter

Parent Board Schematic Design

The green board shown in Figure 10 is called the 'Parent Board'. It interfaces with the IGBT module and two daughterboards- the gate driver and control card. In addition, any interfaces to the enclosure such as sensor or power input connectors are wired through the parent board.

GLV Protection

Overvoltage, undervoltage, and reverse voltage protection are implemented using the LTC4365 IC from Analog Devices [11] . This circuit essentially senses the input voltage and if it is within the valid voltage window, the IC closes the back-to-back MOSFETs (Q1). Conversely, if the input voltage is outside of the valid window, the MOSFETs will not close and the inverter low voltage system will not get power.

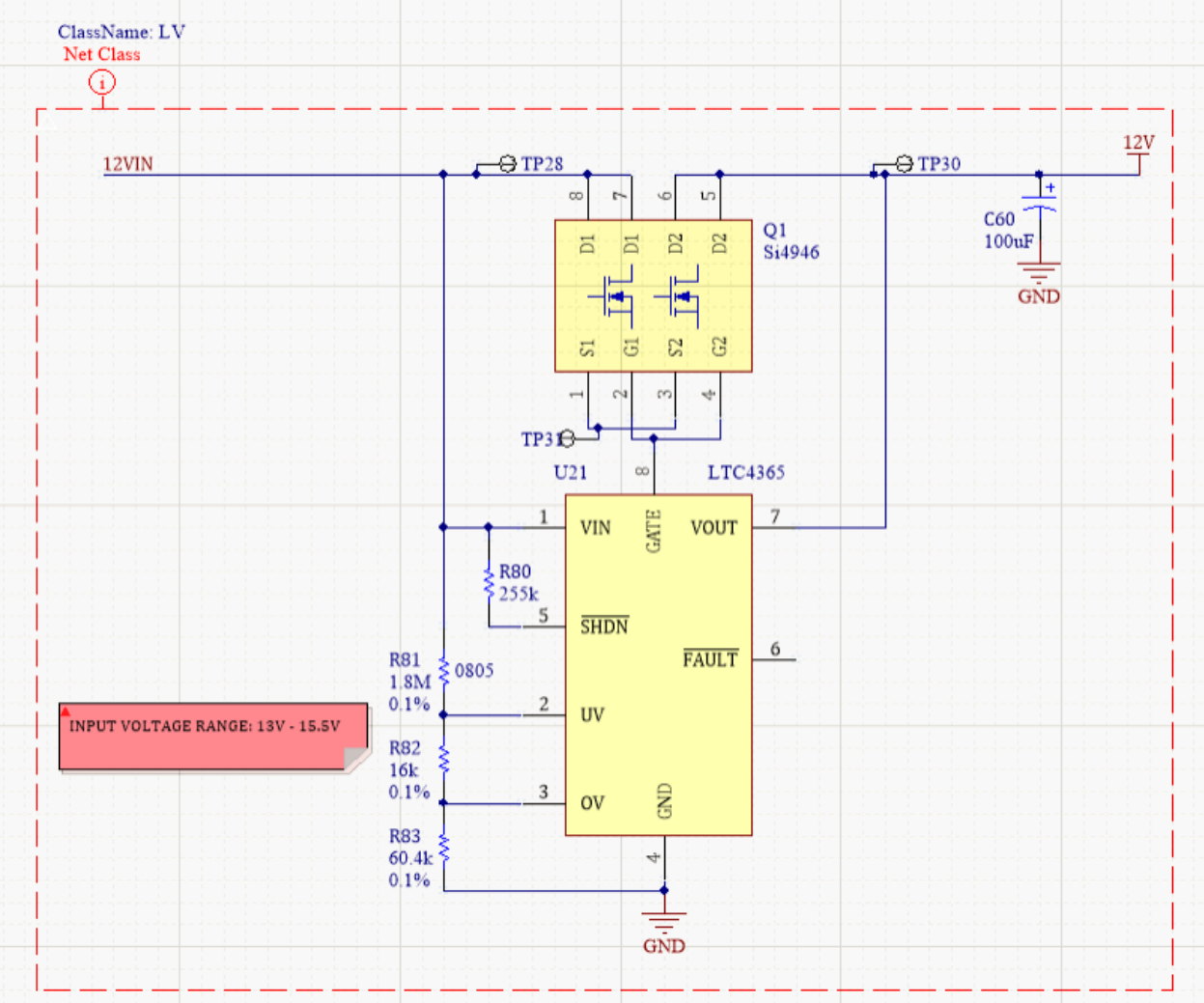

Figure 11: GLV OV/UV/RV Protection Circuitry

There are two comparator inputs that allow configuration of the overvoltage and undervoltage points using an external resistor divider (R81, R82, R83). The comparator reference voltages are internally set to 0.5V so you can calculate the resistor values needed to achieve the desired window of valid voltages. Our desired input voltage range was constrained by the gate driver regulator (IHL0215D15) input voltages. The required input voltage is 13.5V-16.5V for the regulator. This defined the valid voltage range. To check our calculations, we ran a LTSPICE simulation which is shown in Figure 12.

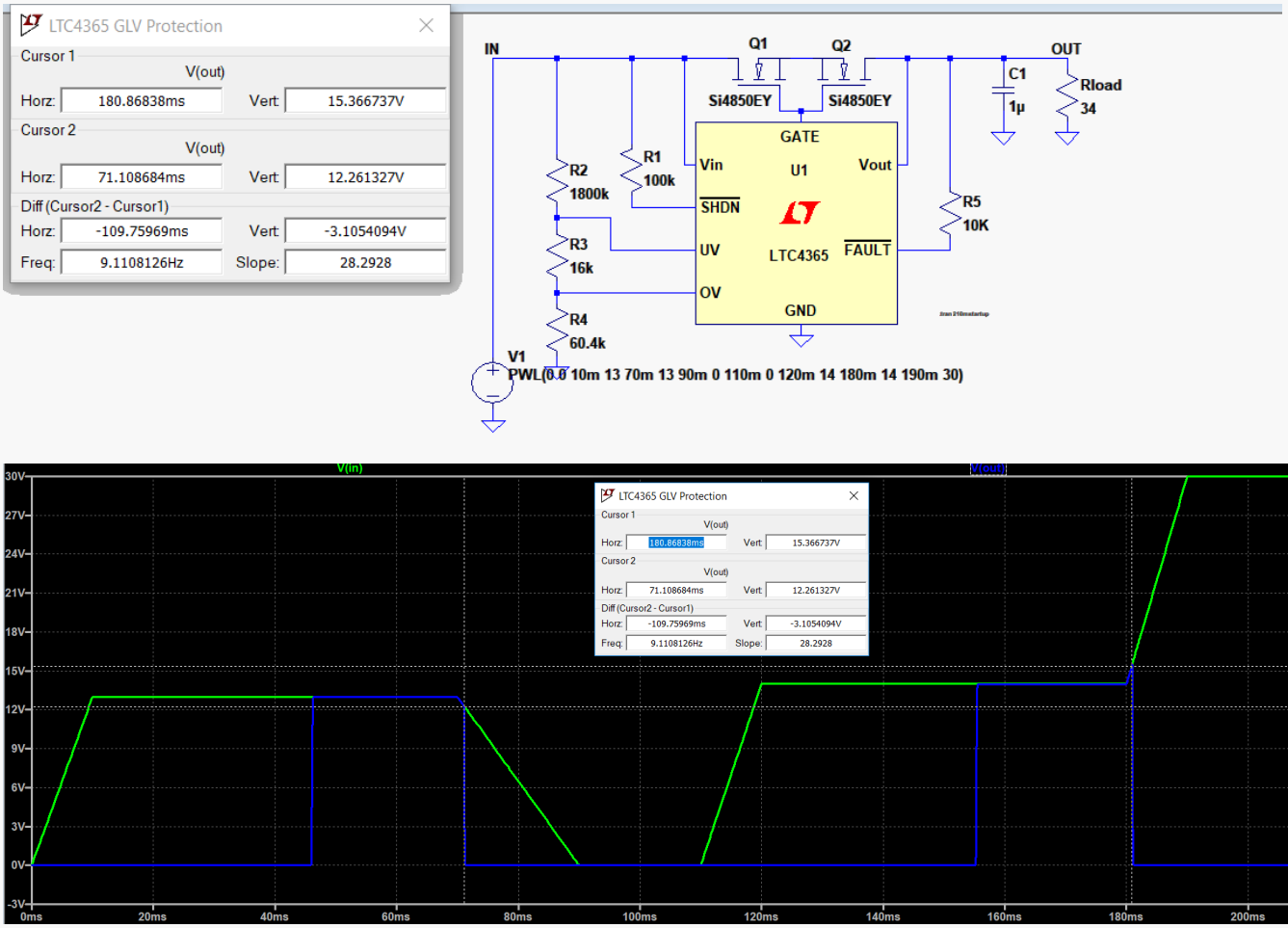

Figure 12: LTSPICE simulation for GLV Input protection

Note that the LTC4365 has a 36ms turn-on delay to debounce live connections and blocks 50Hz to 60Hz AC power. For fast recovery after faults, the LTC4365-1 has a reduced 1ms turn-on delay [8].

Power Supply Circuitry

The parent board holds all the power supply circuitry to generate the voltage rails for all devices on the GLV side of the isolation barrier. A switching regulator (U7) is used to efficiently drop the input voltage of 13.5V-16.5V down to 5V and then a Low Drop Out (LDO) regulator (U6) is used to provide a smooth 3.3V to our MCU and other devices. A dual output precision voltage reference is used to generate a stable 1.65V and 3.3V with 0.05% accuracy. These reference voltages are used in our analog signal conditioning circuitry for DC bus and phase voltage sense so its extremely important that they don't drift.

An isolated power supply (U16) is used to provide 5V on the HV side of the isolation barrier for all the isolation amplifiers in the voltage sense and IGBT temperature sense circuitry. The isolated 0.5V precision voltage reference is used as the excitation voltage for the IGBT NTC temperature sense circuitry.

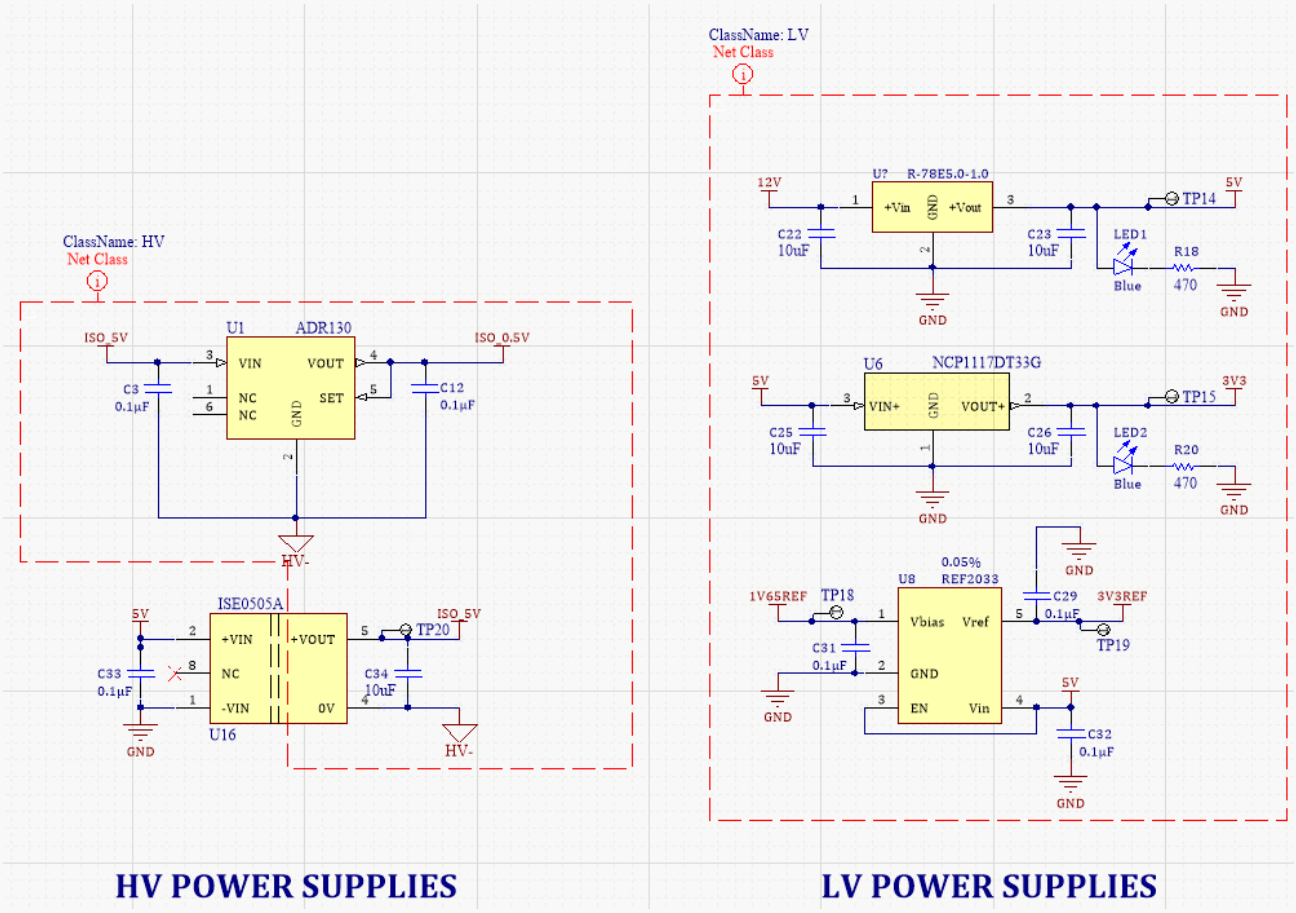

Figure 13: Power supply circuitry

Phase Voltage and DC Bus Voltage Sense Circuitry

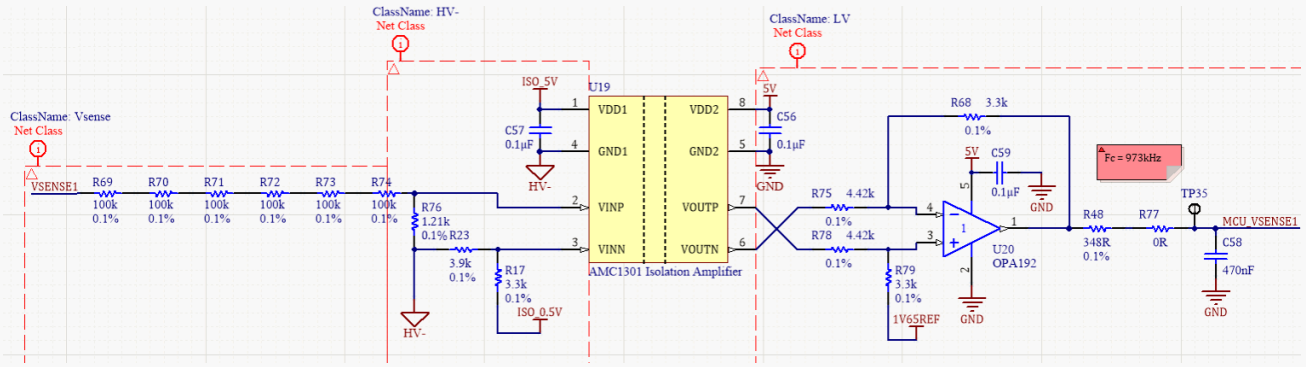

Figure 14: Voltage Sense Circuitry

In order to estimate rotor flux position without an encoder or resolver, InstaSPIN requires sensing of all three phase voltages. The InstaSPIN software requires these signals to arrive at the processor in the form

of an analog voltage. This drove the decision to use the AMC1301 isolation amplifier [12] as the device for isolating the voltage signal. The allowable input voltage between the amplifier pin VINP and VINN is ±250mV. Linearity is not guaranteed for any differential voltage outside of this range. The phase voltage signal is a unipolar signal so an offset voltage created by the R17/R23 voltage divider is used to effectively shift the range to 0-0.5V. The voltage sense range is 0-300V so we now have all the information needed to calculate the resistor values in the divider formed by R69-R74 and R76.

The AMC1301 has a nominal gain of 8.2. Thus, the voltage between VOUTP and VOUTN is –2.05V to 2.05V so VOUT(p-p) for the AMC1301 = 4.10 V. A second op amp (U20) is then used to shift the output signal range so that it is between 0-3.3V.

Due to circuit loading effects, simulation in TINA was used to determine the actual resistor values that offered the best transfer function. It is very important that all the phase voltage sense circuits have nearly identical transfer functions and frequency response so precision low tolerance components were used. Once we built our circuit, we used a frequency response analyzer to ensure that the response had a first-order characteristic (InstaSPIN requirement) and the rolloff was correct. InstaSPIN requires you to input the cutoff frequency [2] so there should only be about 10Hz of variation between the three phase voltage sense circuits.

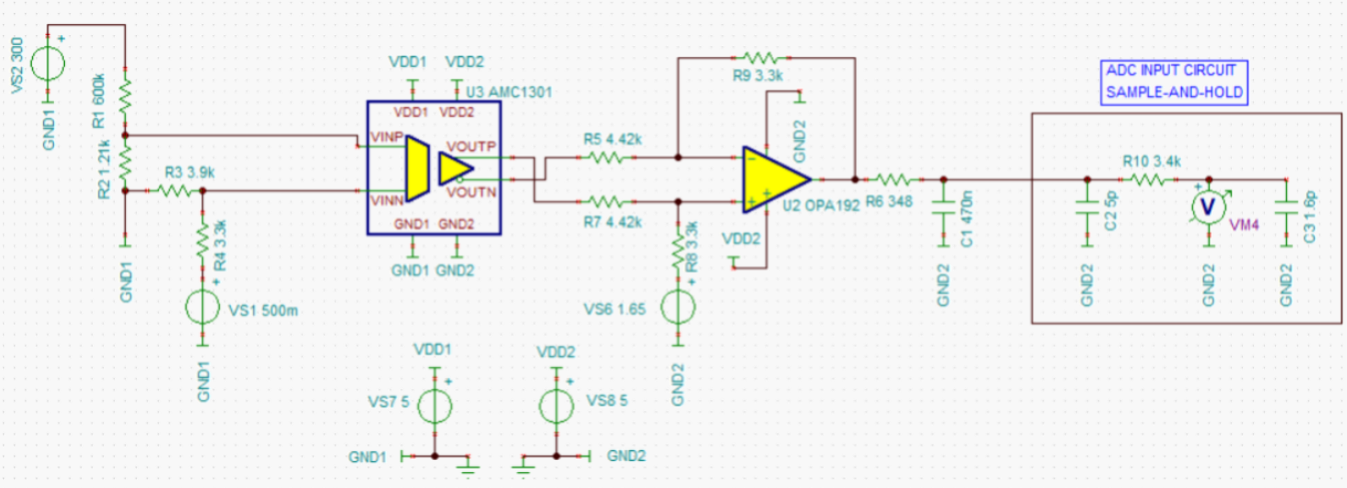

Figure 15: Voltage Sense Schematic for TINA Simulation

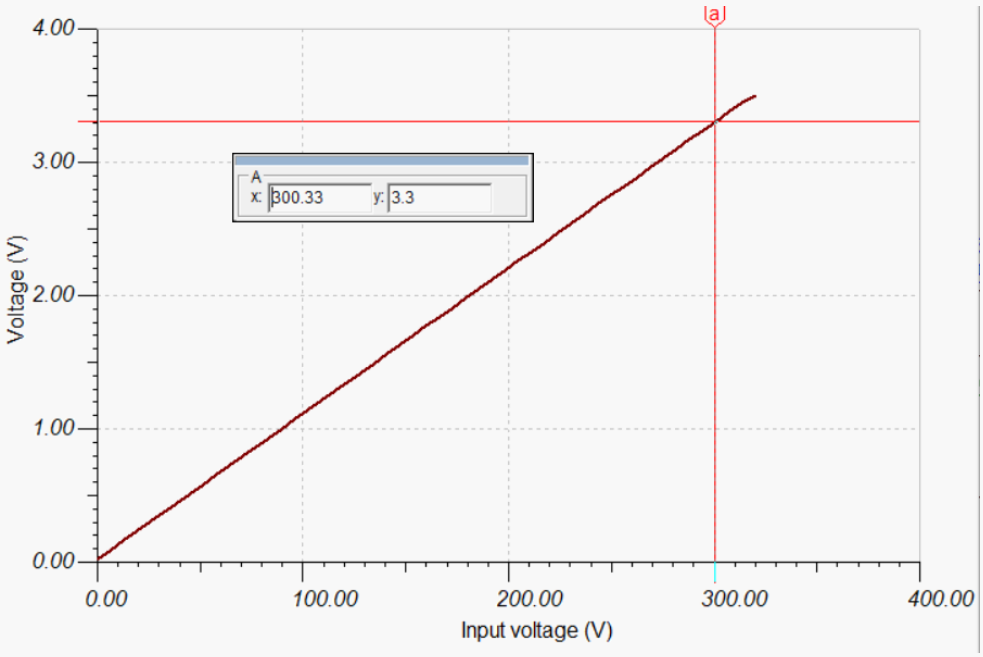

Figure 16: TINA Simulation result for voltage sense circuitry

Isolated IGBT-NTC Temperature Sensing Circuitry

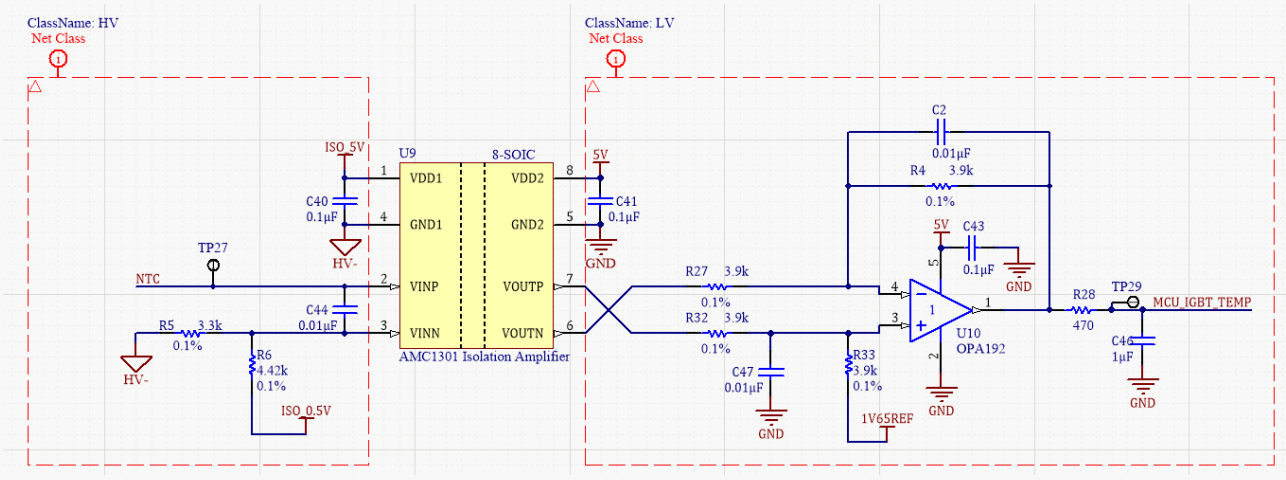

Figure 17: Isolated IGBT NTC Temperature Sensing Circuitry

One of the most critical parameters in power electronic devices is chip temperature. Inside the FS200R07PE4 IGBT module, there is an NTC thermistor mounted in close vicinity to the silicon chips to achieve close thermal coupling. This is crucial information as we can derate phase current to ensure that the IGBT is always in its safe operating conditions (-40°C – 150°C).

Infineon provides the following NTC-thermistor temperature characteristic in the FS200R07PE4 datasheet.

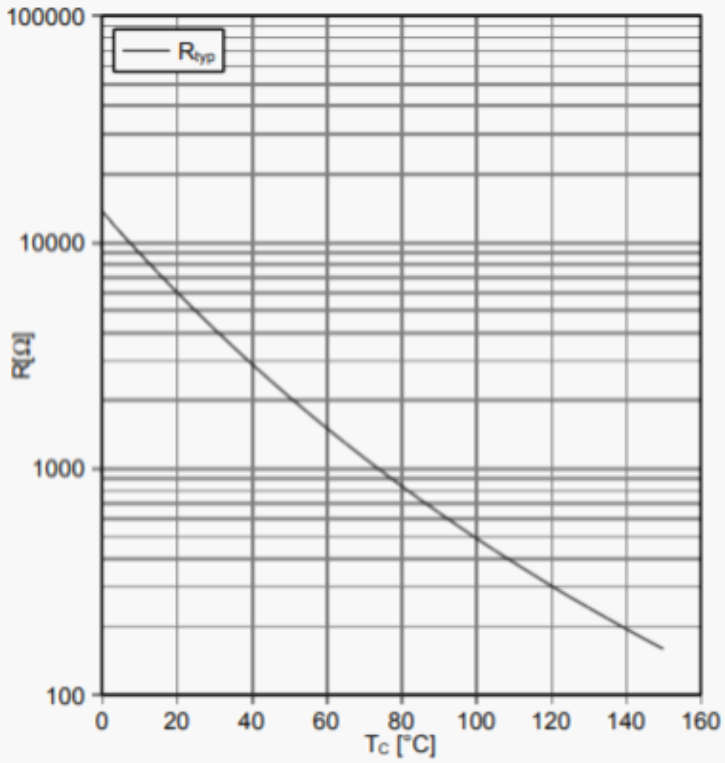

Figure 18: NTC thermistor temperature vs. resistance [4]

From this, we calculated the other resistor needed to utilize the full-scale input range of the AMC1301 isolation amplifier. From Figure 18, you can see the NTC thermistor's resistance changes from about 10k to 200 ohms in the desired temperature range. To maximize resolution in this range, the other resistor (R67) in the divider was selected to be 1.21k as shown below. We set our excitation voltage to 0.5V so there was no way we the signal could go outside the acceptable differential input range on the AMC1301 isolation amplifier.

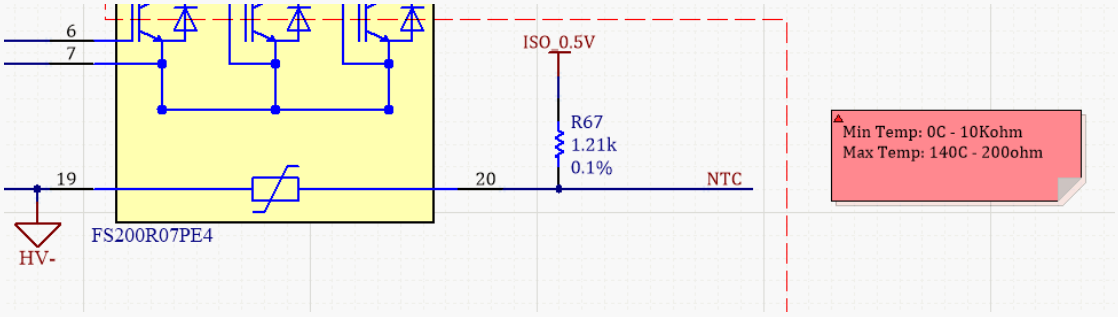

Figure 19: Voltage divider with NTC thermistor

The NTC thermistor meets functional isolation requirements according to standard EN50187. However, the inverter was designed to meet 'reinforced isolation requirements so the NTC signal is galvanically isolated in the same way as the voltage sense signals.

Thermal time constants are long relative to electrical time constants. Heatsinks tend to have time constants measured in 10s of seconds. The NTC baseplate is a bit faster with time constants around 1 of 2 seconds. The junctions are faster with time constants around 50-100ms. We put a 338Hz filter on the final signal that goes to the MCU, but it could be closer to about 100Hz.

Simulation in TINA was again used to validated circuit design and the desired transfer function.

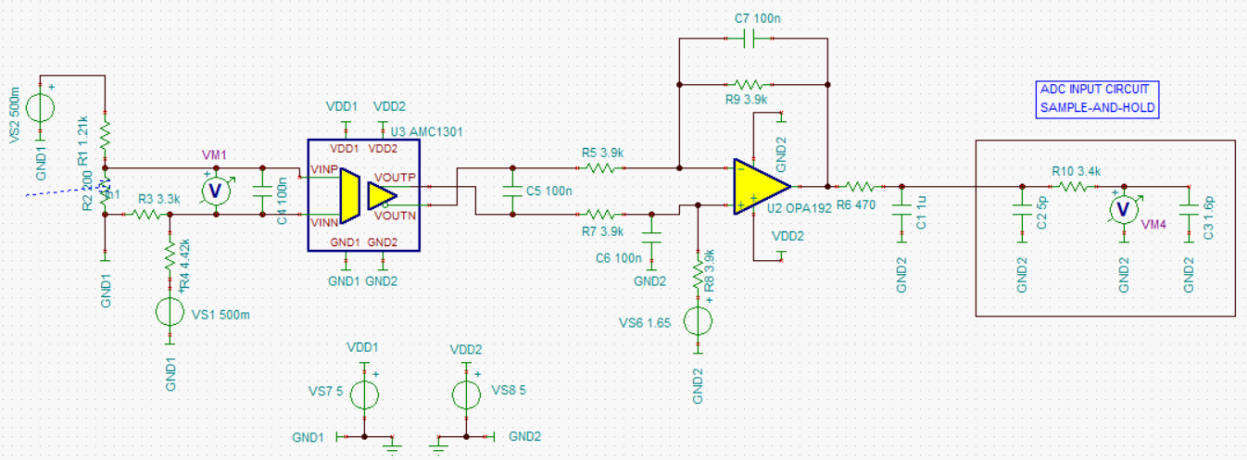

Figure 20: NTC thermistor conditioning schematic in TINA

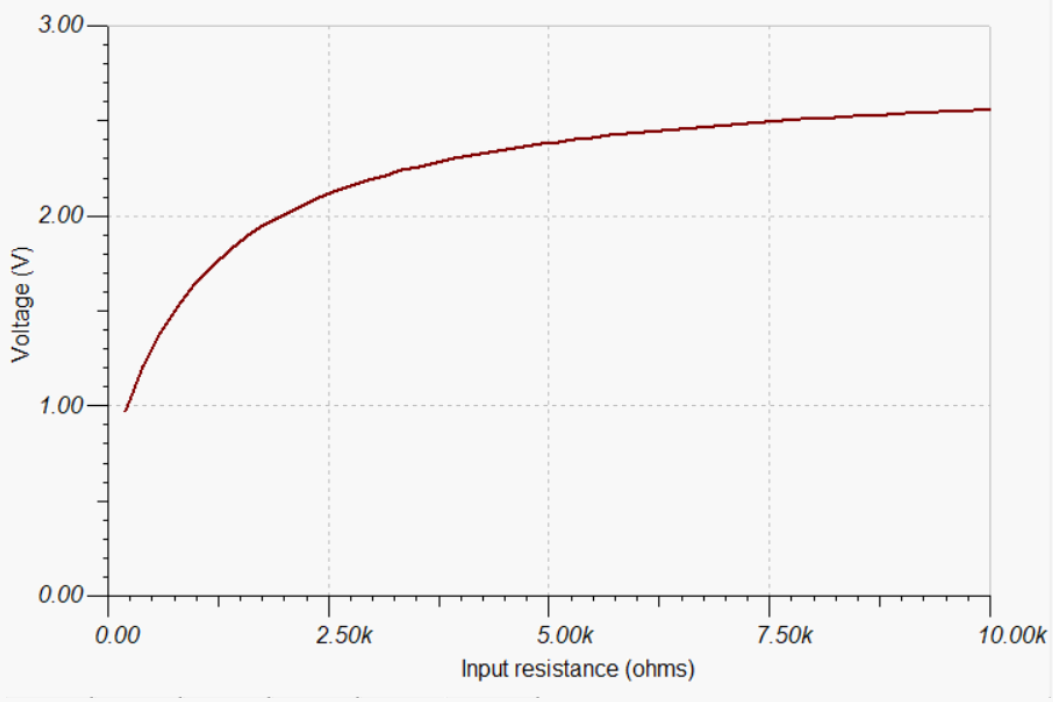

Figure 21: NTC thermsitor conditioning TINA simulation result

As shown by the graph above, the output voltage changes most in the range of 200Ω - 2kΩ, which satisfies our goal of maximizing resolution in the upper end of the temperature range of the IGBT (60°C – 120°C).

Powerstage Circuitry

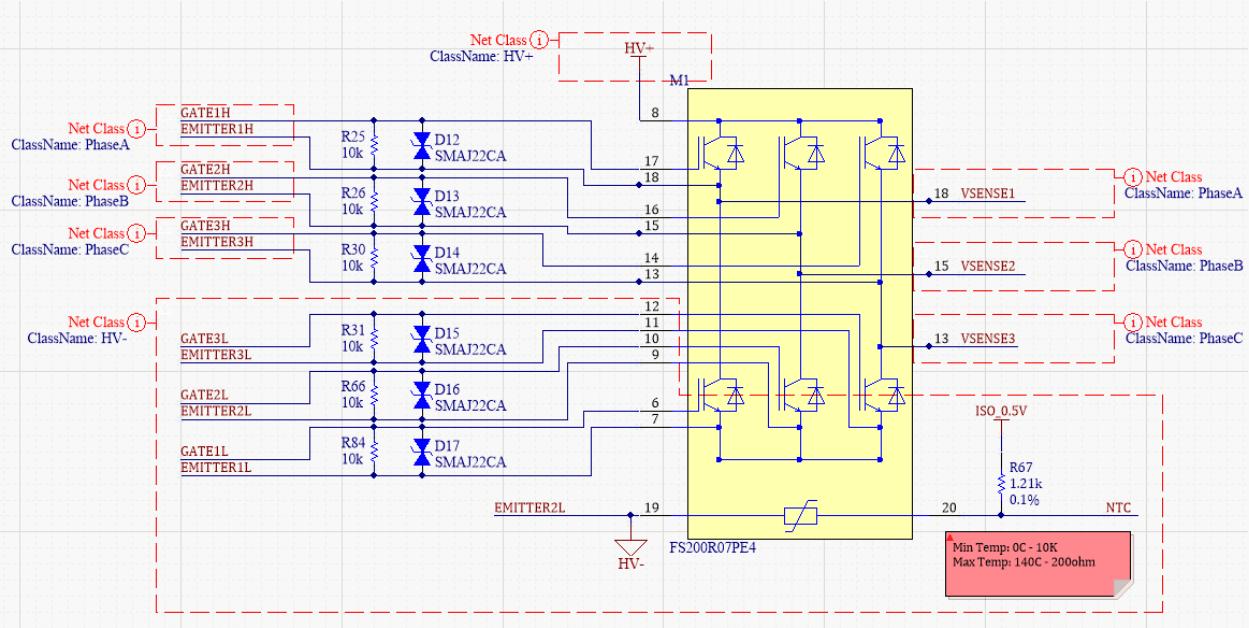

Figure 22: Powerstage circuitry

The powerstage schematic in Figure 22 shows the connections that are made to the IGBT module pins. On the left, we have the six gate-emitter connections for controlling the IGBTs. Notice the that all emitters have a kelvin connection. High di/dt present in the emitter circuit can cause substantial transient voltages to develop in the gate drive circuit if not referenced properly with a kelvin connection.

The bidirectional zener diodes are to protect the gate-emitter from overvoltage. These should be soldered right next to the IGBT pins so there the impedance in that path is minimized.

The 10k pulldown resistors are to protect against unclamped inductive switching conditions. This resistor is especially important for this design since the gate driver is on a separate board. If you don't have this resistor and your gate driver board isn't connected, your IGBT will be damaged when you go to turn on your DC bus. This happened to us.

On the right side of the schematic, we have the three connections for phase voltage sense. Then on the bottom, we have the voltage divider for the NTC temperature sense circuit.

Motor and Capacitor Temperature Sense Circuitry

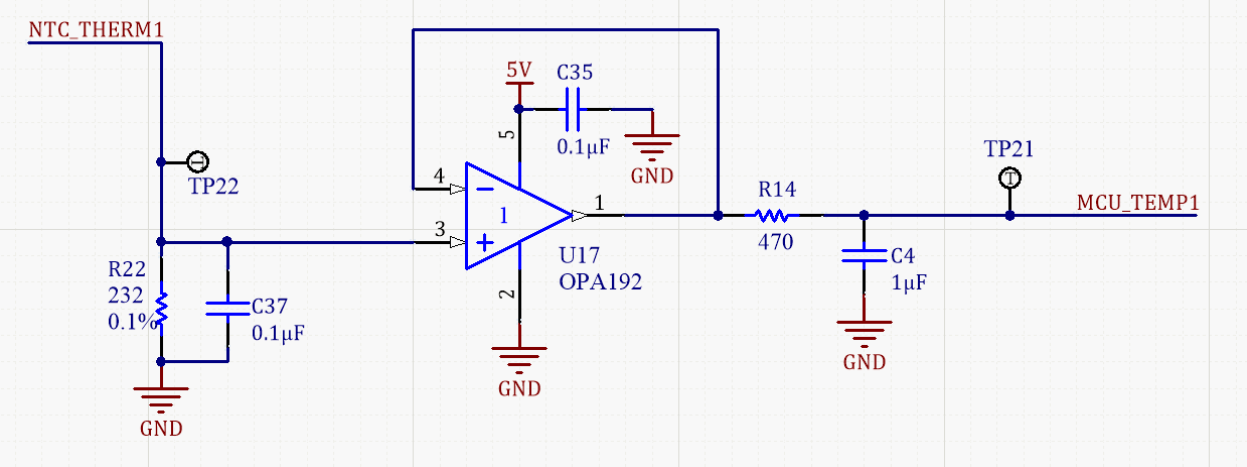

Figure 23: Motor and Capacitor NTC thermistor conditioning circuitry

In each electric motor on the vehicle, there is a thermistor embedded in the motor winding to sense motor temperature. This is absolutely critical to ensure that the maximum temperatures of the winding insulation and internal permanent magnets are not exceeded. Excessive temperatures can lead to damage on the winding insulation and the magnets can become permanently demagnetized.

We included the capability for sensing the case temperature of our DC link capacitors to validate the ripple current rating determined by simulation. Additionally, we can derate phase current appropriately if we see the capacitors are heating up beyond their rated temperature.

To condition the motor and capacitor temperature signals, a simple voltage divider followed by a unity gain buffer is used.

Connectors

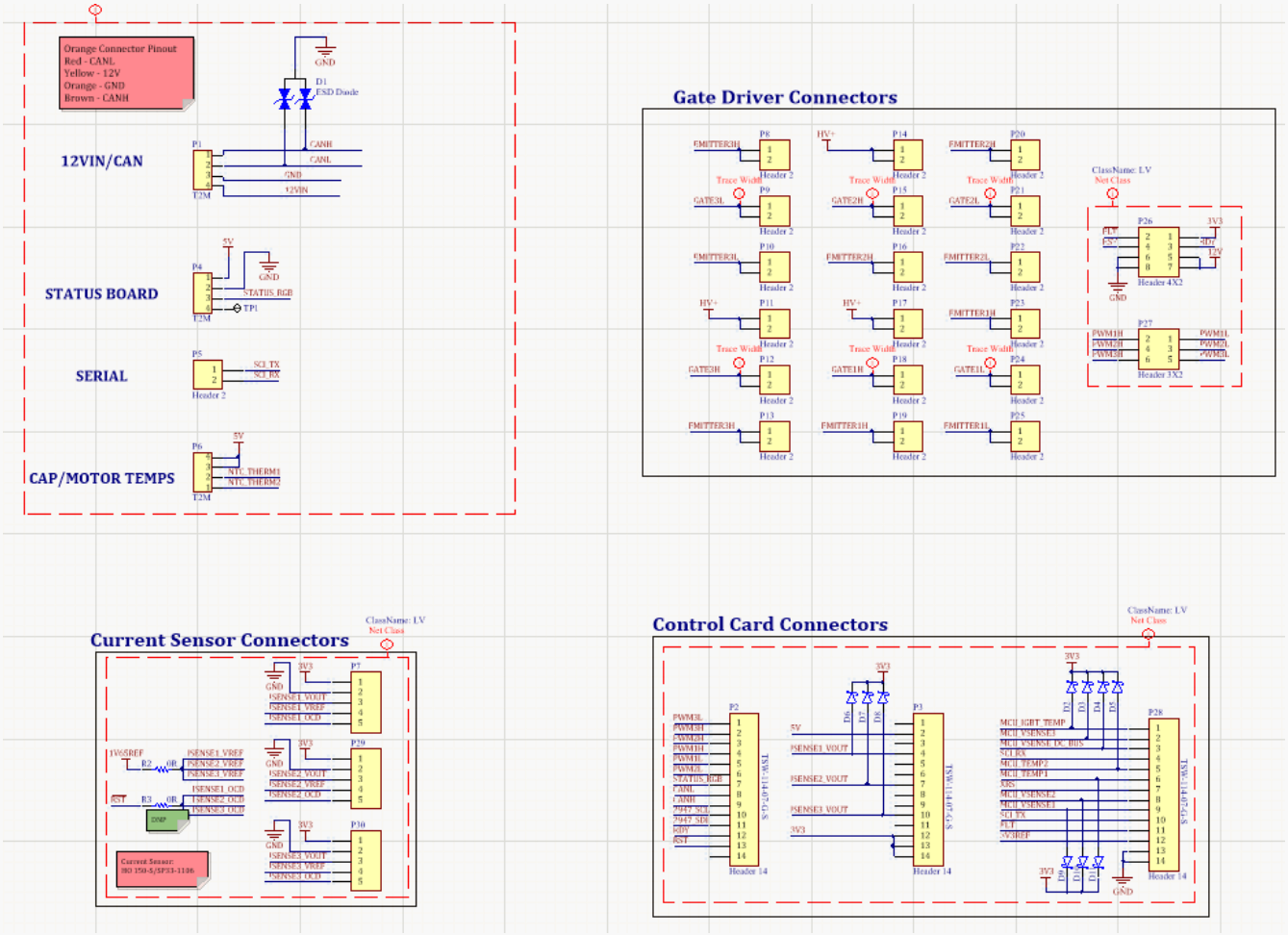

Figure 24: Connectors on parent board

The parent board has connectors for interfacing with the gate driver board, control card, current sensors, and any panel-mount connectors on the case of the inverter. This includes power/CAN, motor temps, and serial (UART) connectors.

To protect against overvoltage on the processor pins connected to the analog inputs, Schottky clamp diodes are used.

Gate Driver Schematic Design

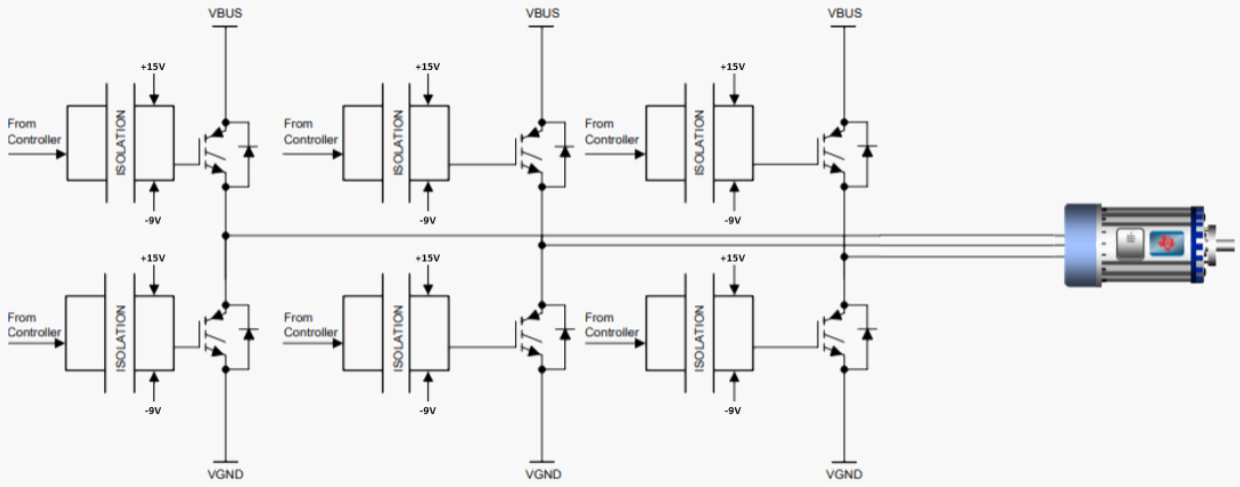

Figure 25: Simplified gate driver circuit for 3phase, 2-level VSI [13]

The gate driver circuit is needed to charge and discharge gate capacitances to switch the IGBT on and off as shown in Figure 26. It is essentially a fancy amplifier that takes the 3.3V PWM signals from the microcontroller and turns them into isolated +15V/-9V PWM Signals. The circuit is the interface between GLV system and the tractive system, providing galvanic isolation between the systems. The gate driver circuit also provides critical safety features like desaturation detection (shoot-through detection) and undervoltage lockout.

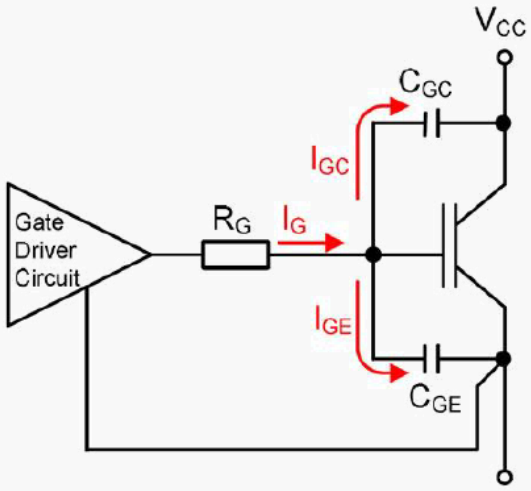

Figure 26: Schematic showing capacitances associated with IGBT gate

Requirements

To optimize packaging and improve component density, we decided to develop our own gate driver. As with all circuit design, the first step we took was to define the circuit requirements.

- Bipolar output (+15V/-9V)
- Vcc: 3.3V – 5V
- Reinforced Isolation
- High CMTI - >50kV/us
- Active miller clamp
- Short propagation delay - <100ns preferred
- Protection features
    - Disable pin to use with hardware overcurrent comparators and MCU safety features
    - Desaturation detection with soft turn-off
    - Input and Output Undervoltage Lockout

After defining the requirements, the next step was selecting a gate driver IC. The ISO5452 from TI [14] satisfied all our requirements and the datasheet was straightforward to understand so we decided to go with that. This was the first time we designed a gate driver so we wanted to keep it as simple as possible. Design to the requirements; nothing more and nothing less.

Gate Voltages

When a voltage is applied to the gate, the gate capacitance is charged and, upon reaching the IGBT threshold voltage (V_{GE_on}), the IGBT turns on and the reverse transfer capacitance (called Miller capacitance) is also charged. To turn off the IGBT, the gate capacitance has to be discharged and, once the threshold voltage (V_{GE_off}) is reached, the reverse transfer capacitance also needs to be discharged.

When a positive voltage is applied between gate and emitter, the IGBT turns on. Due to the IGBT trans-conductance, the collector current is a function of the gate-emitter voltage. There is also a dependency on the saturation voltage. In other words, the higher the gate-emitter voltage, the higher the possible collector current and the lower the resulting saturation voltage. To achieve the lowest possible conduction losses, a high gate-emitter voltage is desired. Manufacturers typically recommend 15V [15].

A negative voltage is typically used to turn the IGBT off because in the case of switching off with 0V, you can get parasitic turn-on and shoot-through can result. This parasitic turn-on can be caused by the feedback effect of miller capacitance or emitter stray inductance. Manufacturers recommend turn-off voltages in the range of -8V to -15V [15].

Power Requirements

Now that we know the voltages required of our gate driver power supplies, we need to know how much power it needs to supply.

$$P_{gate} = P_{driver} + \left(Q_{gate} \times f_{sw} \times \Delta V_{gate}\right) + \left(C_{ge} \times f_{sw} \times \Delta V_{gate}^2\right)$$

$$Q_{gate} = 2.15\mu C \ | \ f_{sw} = 20kHz \ | \ \Delta V_{gate} = 24V \ | \ C_{GE} = 12.0nF \ | \ P_{driver} = 1W$$

$$P_{gate} = 2.17\ watts$$

The IHL0212D1509 isolated dual output DCDC converter [16] was selected as it satisfied the input voltage, output voltages, isolation, and power requirements. 10µF bulk capacitors are used to supply gate current spikes.

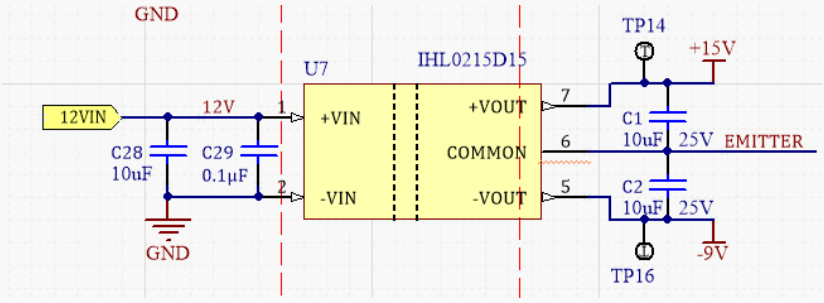

Figure 27: Gate Driver Isolated power supply for generating +15V and -9V

Peak Current Requirements

$$I_{peak\_on\_IC} = 2.5A \ | \ I_{peak\_off\_IC} = 5A \ | \ \Delta v_{gate} = 24V$$

$$R_{GATE\_ON} = \frac{\Delta V}{I_{PEAK\_ON}} = \frac{24\ V}{2.5\ A} = 9.6\ \Omega$$

$$R_{GATE\_OFF} = \frac{\Delta V}{I_{PEAK\_OFF}} = \frac{24\ V}{5\ A} = 4.8\ \Omega$$

$$R_{int,IGBT} = 2\ \Omega \ | \ R_{GD,on} = 4\ \Omega \ | \ R_{GD,off} = 2.5\ \Omega$$

$$P_D = P_{ID} + P_{OD} + P_{OL}$$

where P_D is total power, P_{ID} is total input power, P_{OD} is total output power, P_{OL} is output power under load

$$P_D = 251mW$$

$$P_{ID} = V_{CC1} * I_{CC1} = 5.5V * 4.5mA = 24.75mW$$

$$P_{OD} = (V_{CC2} - V_{EE2}) * I_{CC2} = 15V - (-9V) * 6mA \ = 144mW$$

Solving for P_{OL}, $P_{OL} = P_D - (P_{ID} + P_{OD}) = 251mW - 204.75mW = 82.25mW$

$$P_{OL} = 0.5 \times F_{SW\_MAX} \times Q_G \times (V_{CC2} - V_{EE2}) \times \left(\frac{R_{ON\_MAX}}{R_{ON\_MAX} + R_{GATE\_ON}} + \frac{R_{OFF\_MAX}}{R_{OFF\_MAX} + R_{GATE\_OFF}} \right)$$

Solving for F_{SW_MAX} now,

$P_{OL} = 82.25mW \ \ | \ \ Q_G = 2.15\mu C \ \ | \ \ V_{CC2} - V_{EE2} = 24V$

$R_{ON} = 4\Omega \ | \ \ R_{OFF} = 2.5\Omega \ \ | R_{GATEON} = 3.5\Omega \ \ | \ \ R_{GATEOFF} = 0.3\Omega$

$F_{SWMAX} = 4.9kHz$

4.9kHz is too low! We need 20kHz! This means that a bipolar, non-inverting totem-pole BJT current amplifier must be implemented to buffer current.

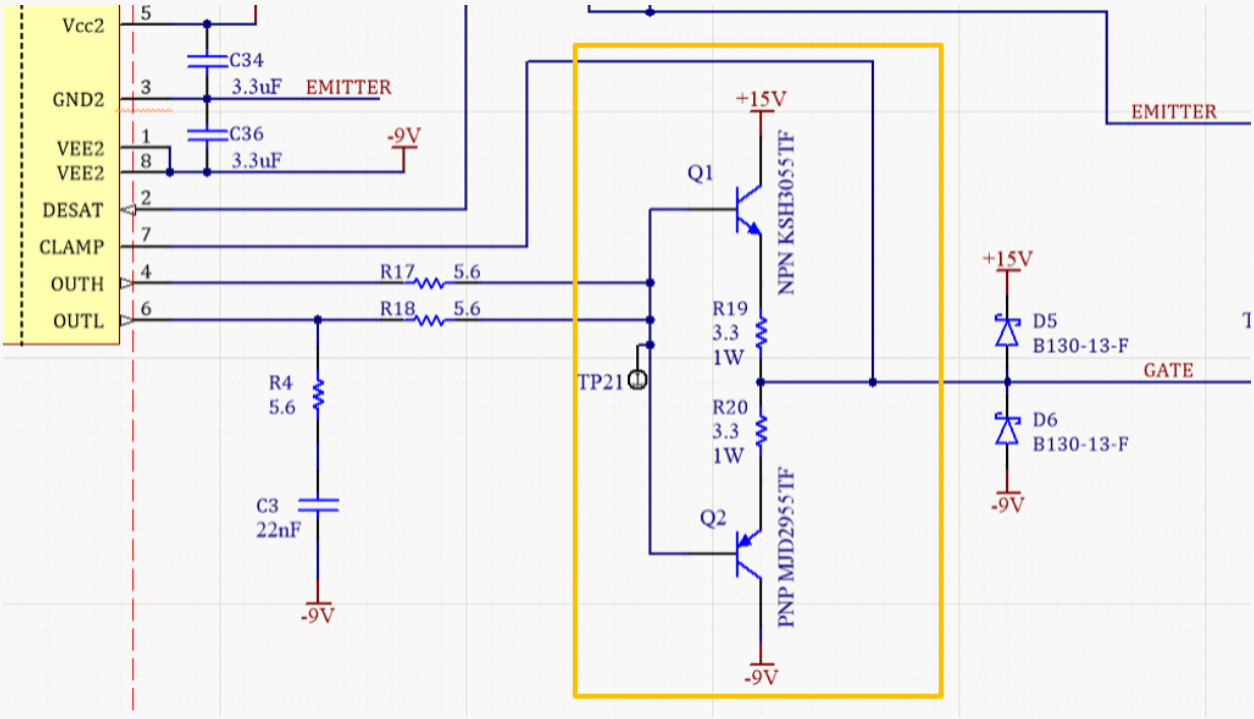

Figure 28: Bipolar, non-inverting totem-pole BJT current amplifier

Desaturation Detection

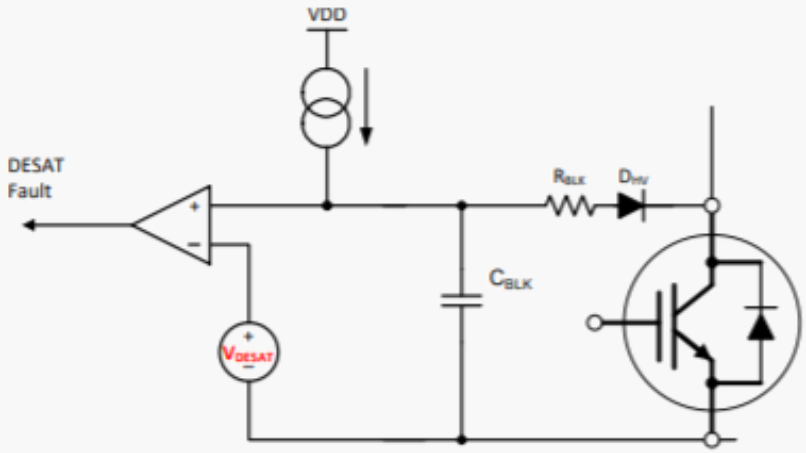

Figure 29: Simplified Desaturation Detection Circuit

The ISO5452 features desaturation detection which is used to detect short circuit events by sensing the voltage across collector and emitter. The circuit consists of a resistor, a blanking capacitor, and a diode. When the device turns on, a current source charges the blanking capacitor and the diode is conducting. The blanking capacitor can be calculated with the following equation.

$$t_{blank} = \frac{C_{blank} * V_{DSTHR}}{I_{charge}} = \frac{200pf * 9V}{0.5mA} = 3.6\mu s$$

During normal operation, the blanking capacitor voltage is clamped at the forward voltage of the device. However, when a short occurs, the capacitor voltage is quickly charged to a higher voltage and once it exceeds the internal 9V desat threshold, a soft turn-off procedure will initiate which will open the IGBTs in a controlled manner over 1-2µs [17]. If you were to "hard turn-off" the IGBT during a short circuit event, the collector-emitter voltage will rise due to parasitic inductances and likely damage the switch. Because we added in the totem pole amplifier, we need to implement an additional RC network for soft-turn off to work correctly.

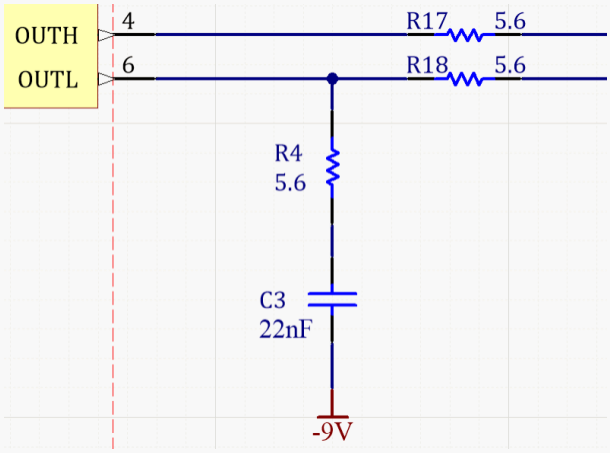

Figure 30: Additional RC network to implement soft turn off of IGBT

To avoid false desat triggering, fast recovery diodes with low capacitance are used (D2, D3). We used the BAV3004W-7-F which has a blocking voltage of 300V and reverse recovery time of 50ns [18]. The complete desaturation detection circuit is shown in Figure 31.

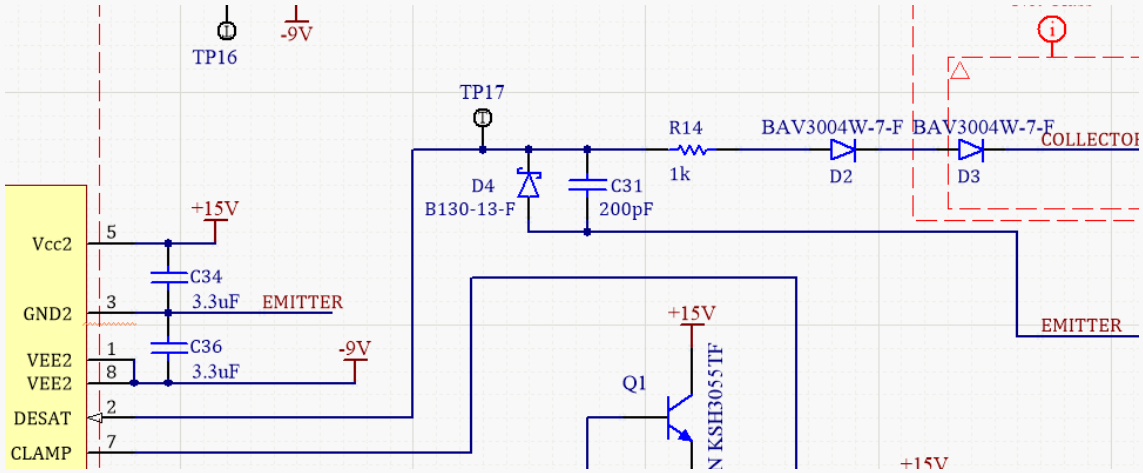

Figure 31: Complete desaturation detection circuit

Gate Resistor Selection

Initially, we selected the lowest recommended gate resistor (3.3Ω) because we wanted to minimize IGBT turn-on and turn-off times and in turn switching losses. However, after our first round of dyne testing, we saw oscillatory spikes in the gate-emitter circuit, which caused a host of EMI problems and stress on our IGBTs. This oscillatory ringing indicates that the RLC circuit underdamped and that there is too much inductance in the gate-emitter loop We increased our gate resistance to 12 ohms to add more damping to the system and no longer saw any ringing on the gate. Of course, the switching losses increased but

we could reject the heat so that was not a problem. If gate-emitter inductance was reduced, the gate resistor value could be reduced.

GLV Side of Gate Driver

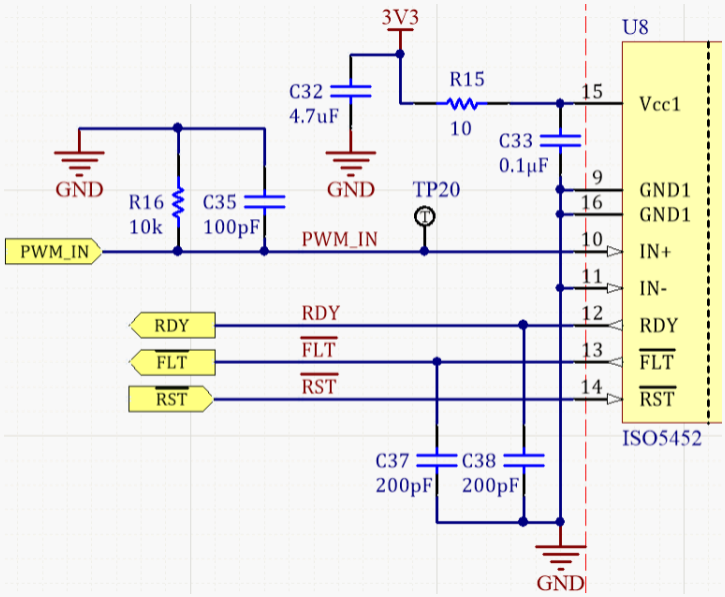

Figure 32: GLV Side of Gate Driver

The GLV side of the gate driver is very straightforward. It is supplied with 3.3V with a 4.7µF bulk and 0.1µF decoupling capacitor. The PWM line has a 10k pulldown resistor to ensure the IGBT goes to an off-state when the PWM line isn't driven. When the R/S/T/ pin is pulled low, this will disable the outputs of the gate driver. Thus, we have a common open drain fault bus connected to R/S/T/ that ORs the signals from the overcurrent comparators, overvoltage comparator, and the fault pins on the MCUs. If any signal pulls low, all gate drivers will disable their outputs.

Complete Gate Driver Circuit

The complete gate driver circuit is shown in Figure 33. The difficult part of a gate driver is not circuit design, but rather in the layout. This is discussed in the layout section.

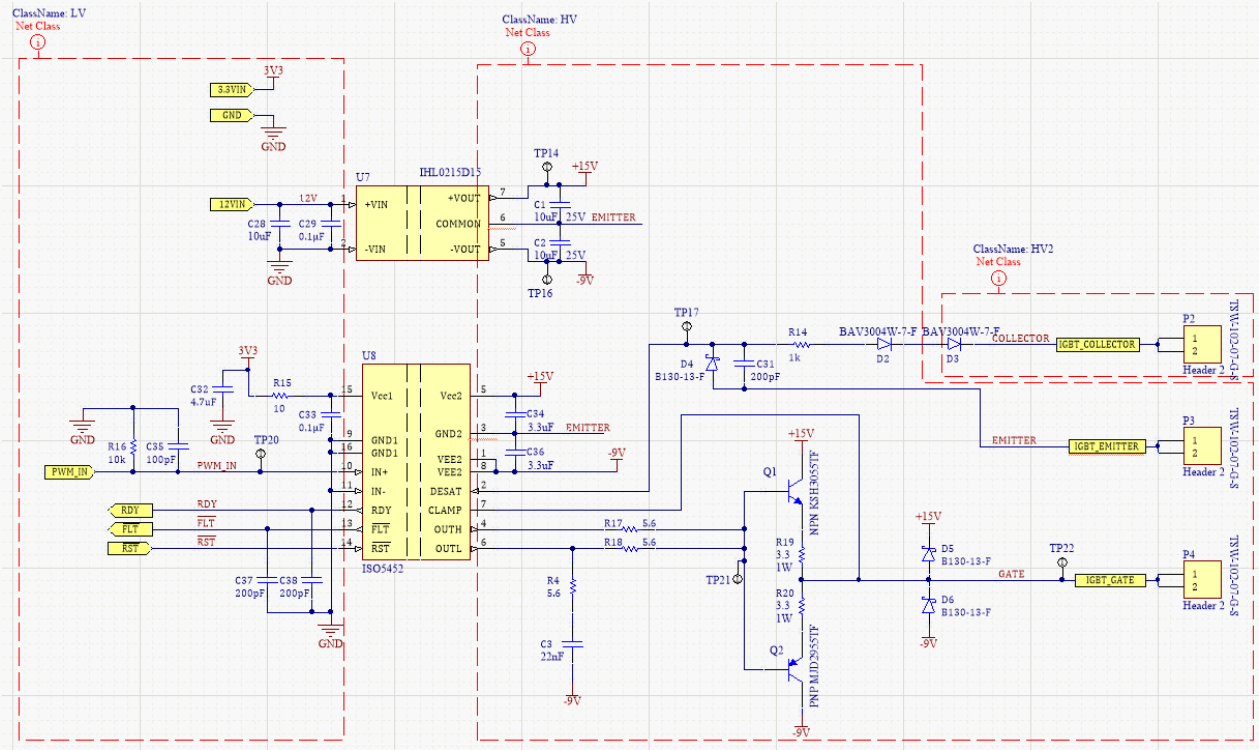

Figure 33: Complete gate driver schematic

Control Card Schematic Design

DSP Selection

The control card holds the DSP (TMS320F28069F) and the hardware overcurrent protection circuitry. We discussed this in the Architecture section, but the TMS320F28069F is the highest performing processor that is InstaSPIN enabled [3].

The inputs and outputs going to and from the control card are listed below in the table. All I/O have low pass filters to help keep 10MHz+ EMI from the power stage from getting into the low-voltage logic. Note that the phase voltage sense do not have this filter populated in order to preserve the first order response that is required by InstaSPIN.

Inputs	Outputs
Analog • Three phase current signals • Three phase voltage signals • DC bus voltage • IGBT temperature Digital • Gate drivers FLT bus • Gate drivers RDY bus • JTAG programming lines • CAN • UART serial • External processor reset signal	• Status RGB digital signal • Six HRPWM to gate driver • Overcurrent comparator to gate driver • Bus overload comparator to gate driver • CAN • UART serial • Programmable reset to gate driver

A power LED is present that indicates when 3.3V power is present. An orange debug LED is included as well.

Programming the DSP

To program the Piccolo chip, we primarily used a CAN bootloader created by Beat Arnet from C2Prog. This is extremely useful as we can program each individual microcontroller by simply accessing the CAN bus. Otherwise, the chip can be programmed via JTAG which is broken out to a connector (P3).

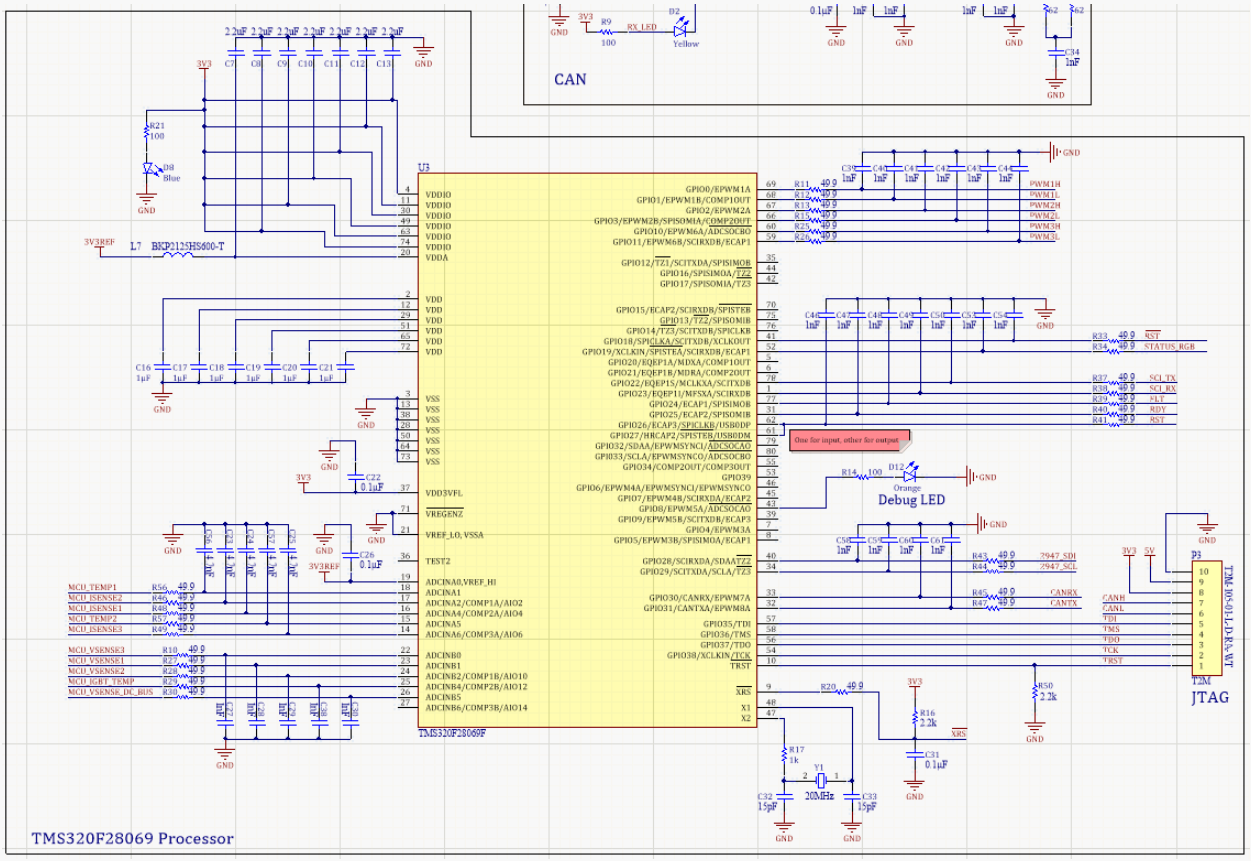

Figure 34: TMS320F28069 processor and accommodating circuitry

CAN Transceiver Circuitry

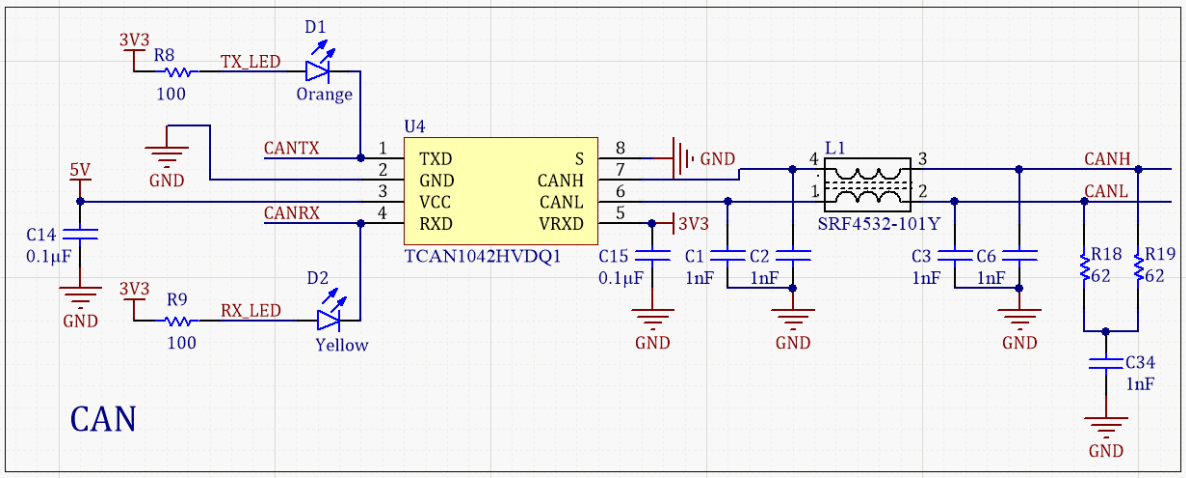

Figure 35: CAN Transceiver circuitry

The CAN bus circuitry was designed with reliability and high signal integrity as the highest priorities. Thus, the circuit is very robust to EMI. To filter out common mode noise, we utilize split termination and a

common mode choke (CMC). To filter out differential noise, we have filter caps on both CAN-lines before and after the CMC. The CAN transceiver (U4) is one of the most robust transceivers sold by TI [19]. It has a very high common mode input voltage range and has bus fault protection up to ±70V. There are LEDs in parallel with the CAN lines to indicate when there is communication on the lines. The termination resistor should be populated only on the node with the longest stub length.

Bus Overload Circuitry

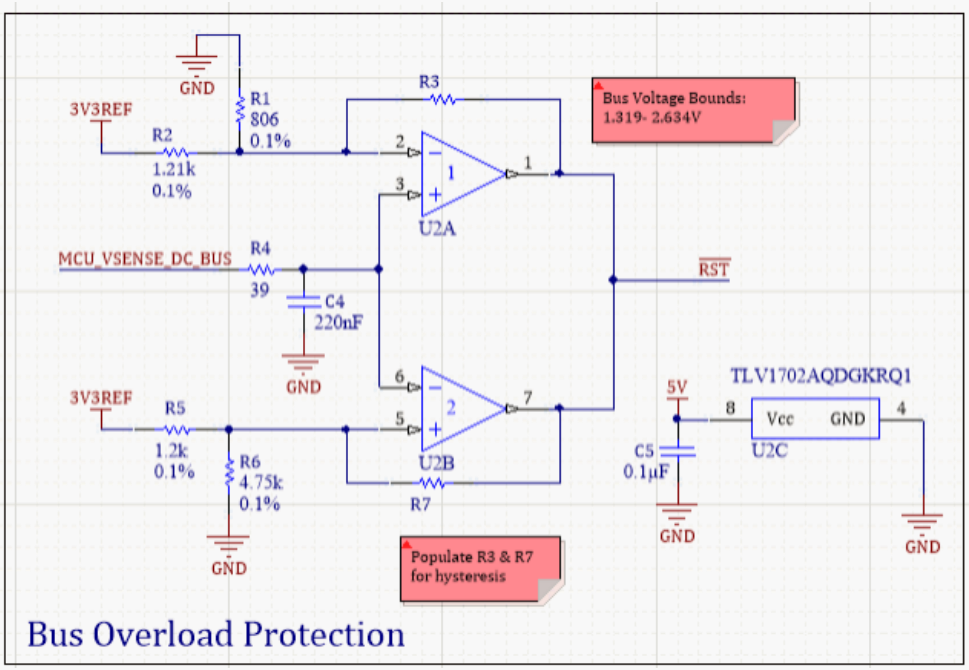

Figure 36: DC Bus Overload Detection Circuitry

A windowed comparator is used to set the bounds for minimum and maximum allowable bus voltage. The comparator bounds are 1.319V – 2.634V, which corresponds to 150V – 300V on the DC bus. If the bus is outside of this range, the IGBTs will be opened.

Note it is very important that precision components are used to set the windowed comparator bounds as these are very sensitive signals. 0.1% tolerance resistors and high accuracy voltage references are used.

Hardware Overcurrent Detection Circuitry

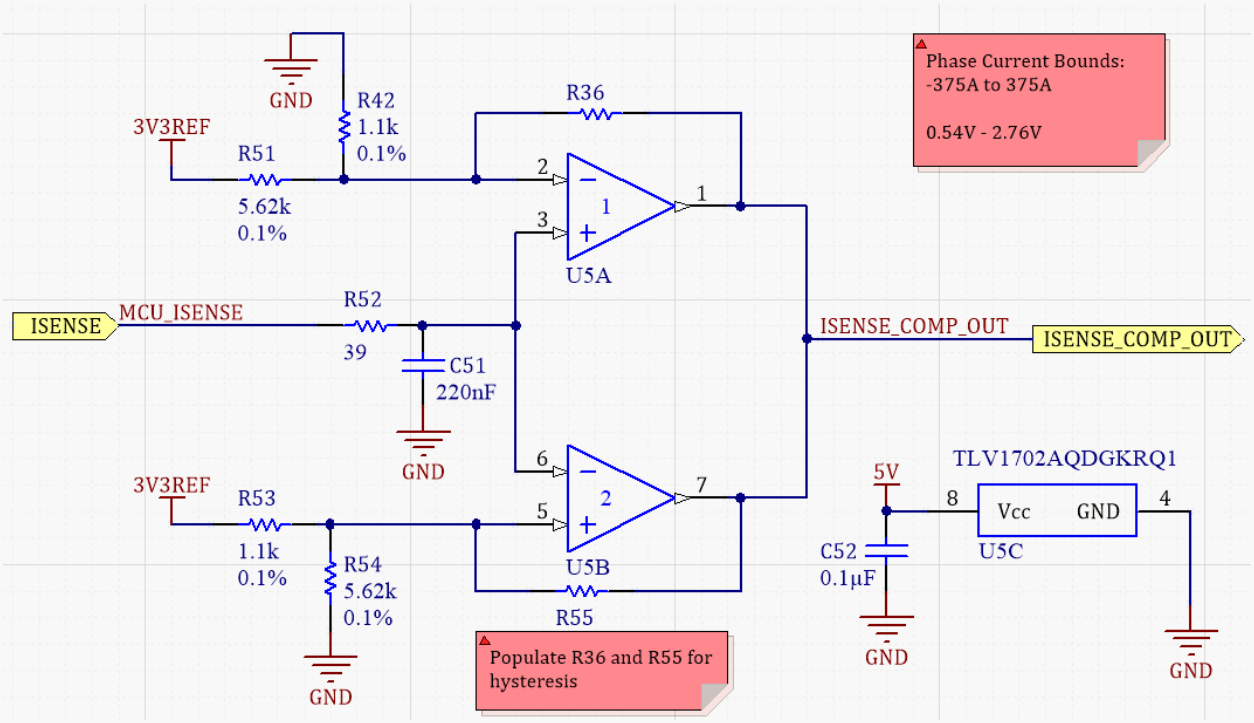

Figure 37: Hardware overcurrent detection circuitry

The circuitry is nearly identical to the bus overvoltage circuit shown above. The only difference are the resistors used for setting the bounds of the valid voltage window. Anything outside of -375A – 375A (0.54V – 2.76V) is considered an overcurrent event.

PCB Layout Considerations

Parent Board Layout

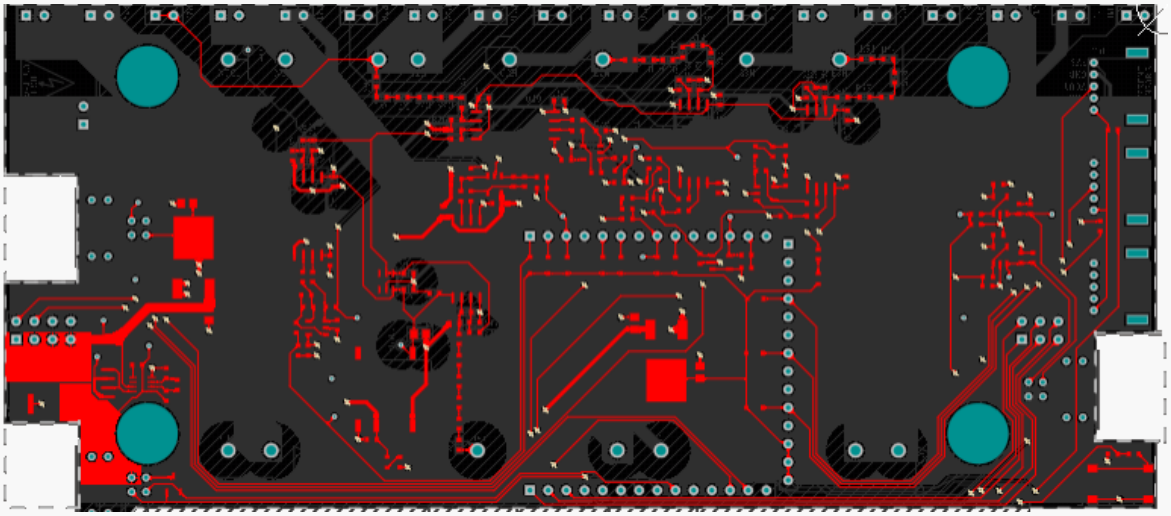

Figure 38: Parent board - top layer

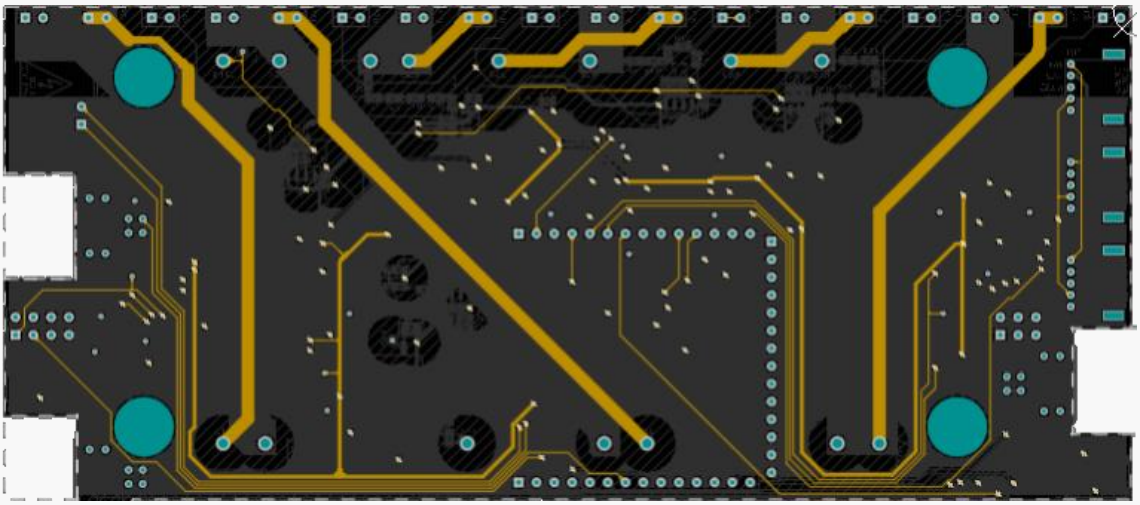

Figure 39: Parent board - mid layer 1

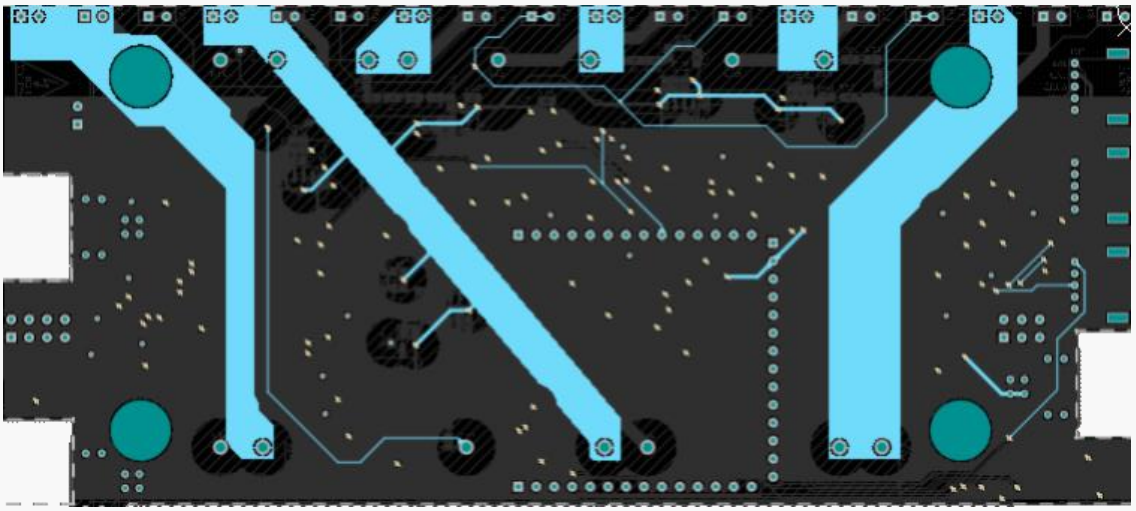

Figure 40: Parent board - mid layer 2

Figure 41: Parent board - bottom layer

Gate Driver Layout

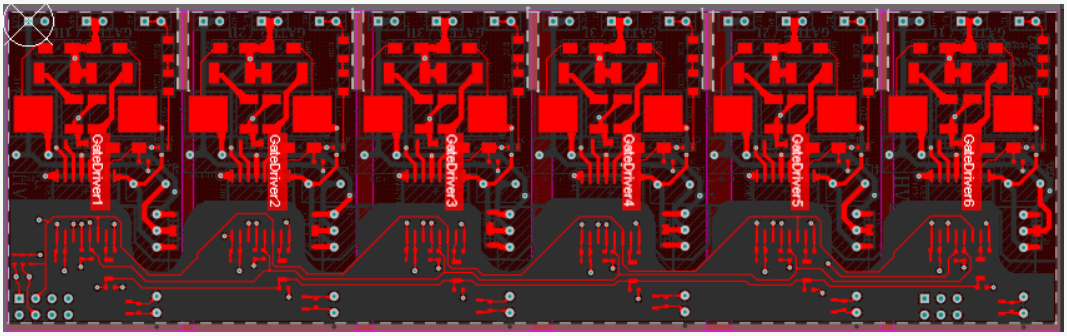

Figure 42: Gate Driver - top layer

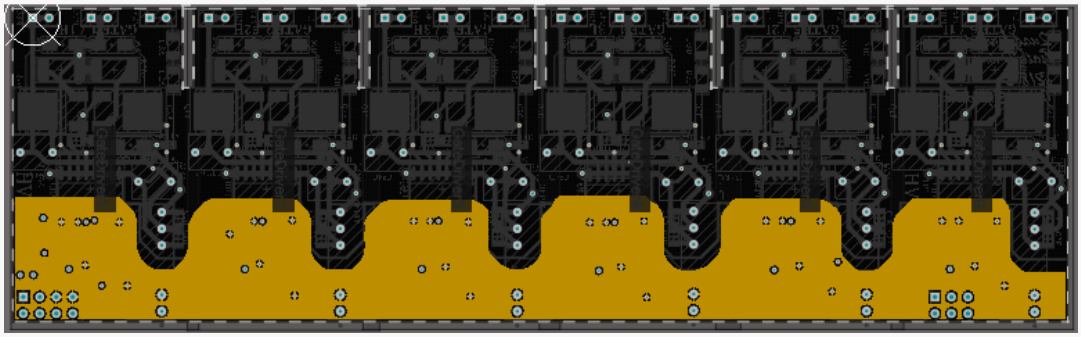

Figure 43: Gate Driver - Mid layer 1

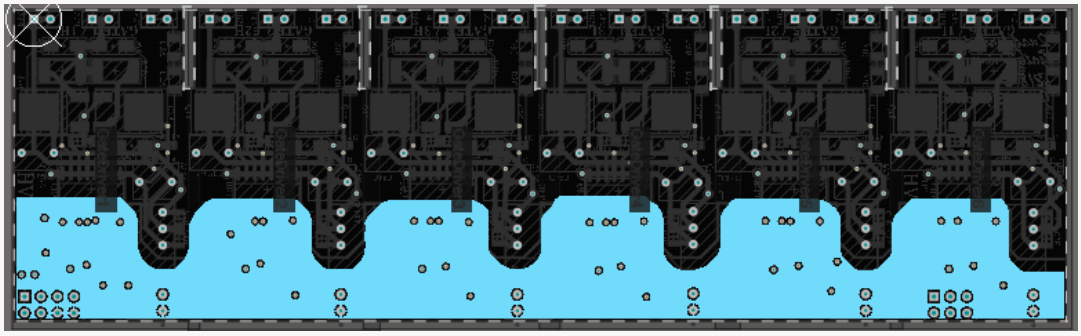

Figure 44: Gate Driver - mid layer 2

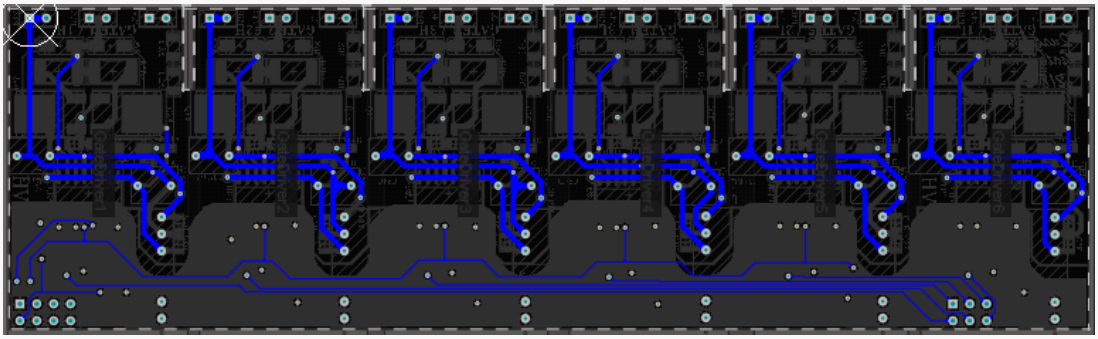

Figure 45: Gate Driver - bottom layer

Control Card Layout

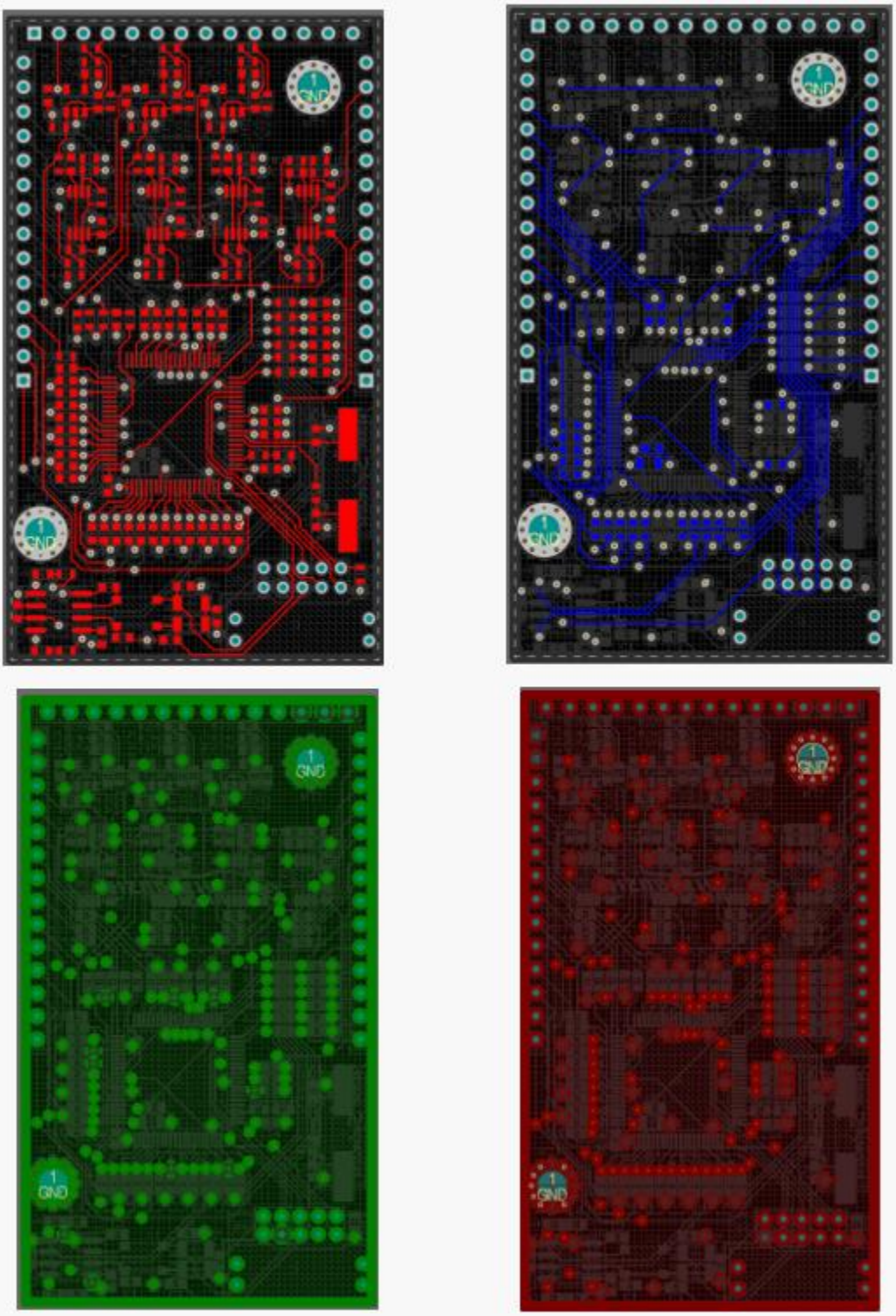

Figure 46: Control Card PCB Layers

Isolation Requirements

To ensure proper isolation between the high voltage and low voltage systems, the FSAE rules [1] state the following requirements for PCB spacing.

Required spacing are as follows:

Voltage	Over Surface	Thru Air (Cut in board)	Under Coating
0-50VDC	1.6 mm (1/16")	1.6 mm (1/16")	1 mm
50-150VDC	6.4 mm (1/4")	3.2 mm (1/8")	2 mm
150-300VDC	9.5 mm (3/8")	6.4 mm (1/4")	3 mm
300-600VDC	12.7 mm (1/2")	9.5 mm (3/8")	4 mm

Our maximum bus voltage is 252V and we conformally coat all our boards so that means we needed 3mm of clearance between all HV and LV tracks. To implement clearances in Altium, we created HV and LV net classes and then defined clearance constraints between those net classes. For example, take a look at the isolated NTC temperature sense circuit shown in Figure 47.

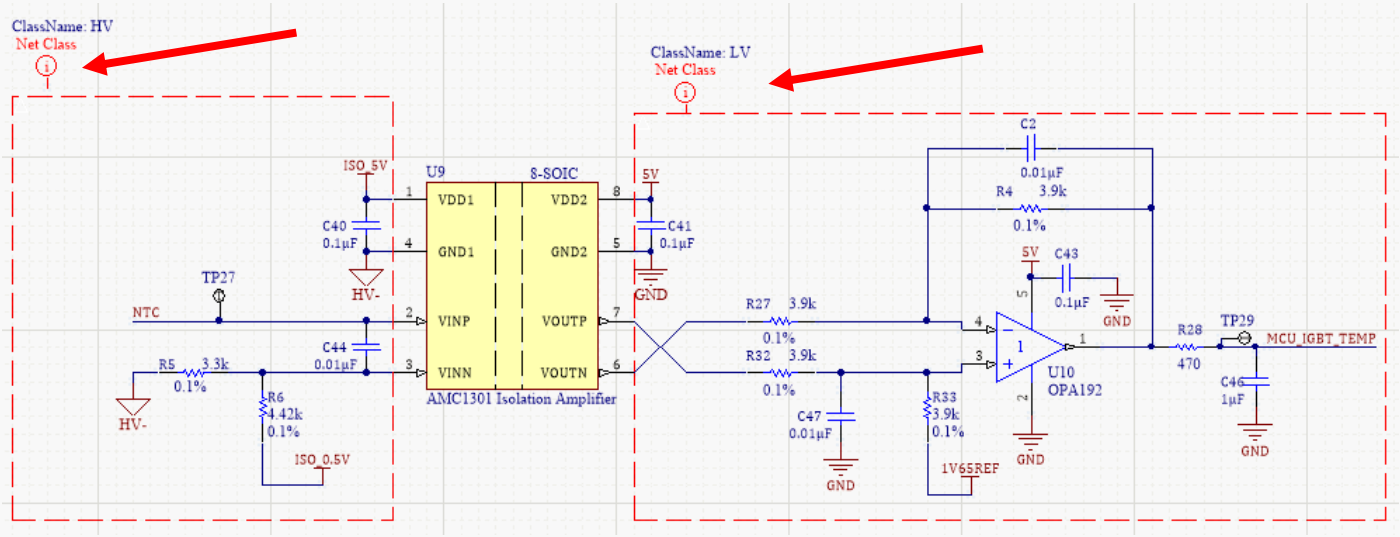

Figure 47: Schematic showing net classes used for implementing isolation

On the left, every node that lies inside the blanket belongs to the 'HV' net class. Similarly, every node that lies inside blanket on the right belongs to the 'LV' net class. Then, in the design rules, we created new clearance constraints that says, "any net belonging to the 'LV' class must be 3mm away from any net belonging to the 'HV' class".

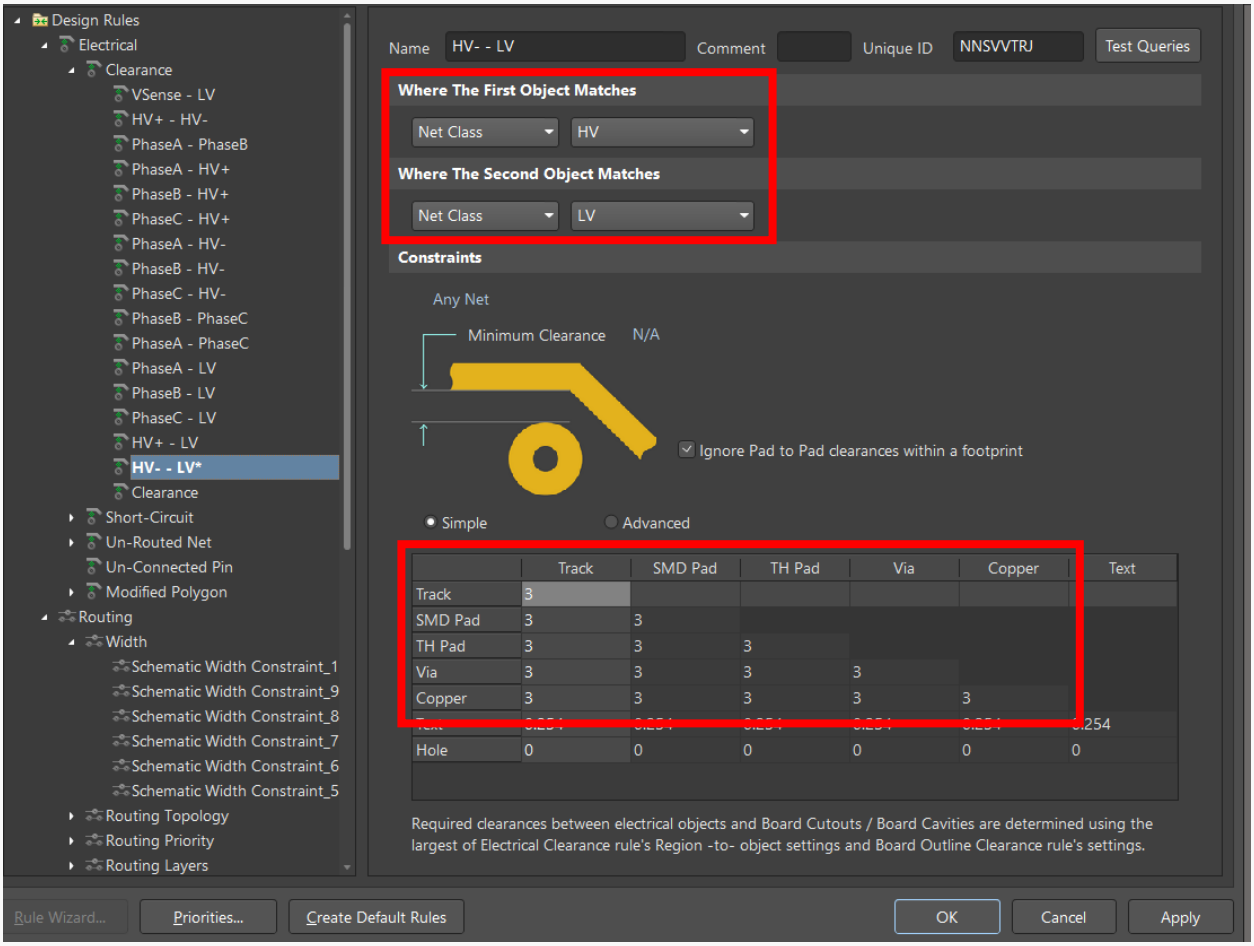

Figure 48: Altium PCB Clearance rules for Isolation Requirements

These clearance constraints were created not only for isolation between HV and LV, but also for any nets that may have a ΔV of 50V+ such as HV+ to HV-.

Gate-Emitter Inductance Layout Considerations

The gate drive circuit can be modeled as the following RLC circuit shown in Figure 49.

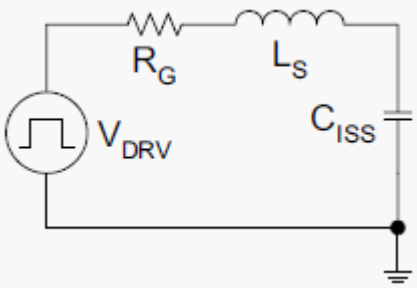

Figure 49: Gate Drive Circuit Model

At the beginning of the switching transition, the gate current increases very rapidly. That current must flow through the parasitic inductance in the PCB trace and will be slowed down depending on how large the inductance value is. As a result, the turn-on and turn-off delay gets longer because the time required to charge/discharge the input capacitance gets longer. Additionally, the gate inductor and capacitor form a resonant circuit. If the inductance is too large and there is not enough damping from R_G, the gate signal will resonate, resulting in voltage overshoot and ringing on the gate. This ringing effect can potentially damage the device from overvoltage and can also cause a significant amount of conducted or radiated noise [15].

To reduce ringing on the gate, there are two approaches you can take.

1) Increase gate resistance (damping)
2) Decrease gate inductance

The first approach is more of a "band-aid solution" and is not ideal as it will increase switching losses. When designing a PCB, the gate inductance should be as small as possible. Lenz's law states

$$v(t) = -\frac{d\Phi(t)}{dt} \quad L = \frac{\Phi(i)}{i}$$

Magnetic flux is proportional to loop area, so the inductance of a circuit depends on the geometry of the current path. Thus, to reduce inductance in the gate-emitter loop, you want to do two things.

1. Reduce loop length/area – minimize trace length and traces should be adjacent
2. Make traces as wide as possible

Note: With our current design, the gate-emitter inductance is not optimized, and we needed a relatively high gate resistors in order to compensate for this. This is because the gate driver lives on a daughter-board so the gate-emitter loop is quite long. In the next revision, the gate driver circuit will be placed right next to the IGBT gate in order to reduce this.

Capacitive Coupling Layout Considerations

Any conductors separated by a dielectric such as air have capacitance between them. If there is a change of voltage on one, there will be an induced current in the other equal to

$$i = C\frac{dV}{dt}$$

This is particularly important in inverters because you are switching high voltages very quickly. For example, in our inverter, we have terminals swinging back and forth between HV+ and HV- at 10kV/µs. If there is 10pF of capacitance between a track connected to a motor terminal and a plane at HV-, that plane would develop 100mA transients. That's a lot of noise to contend with and if that gets back into the gate circuit, bad things can happen.

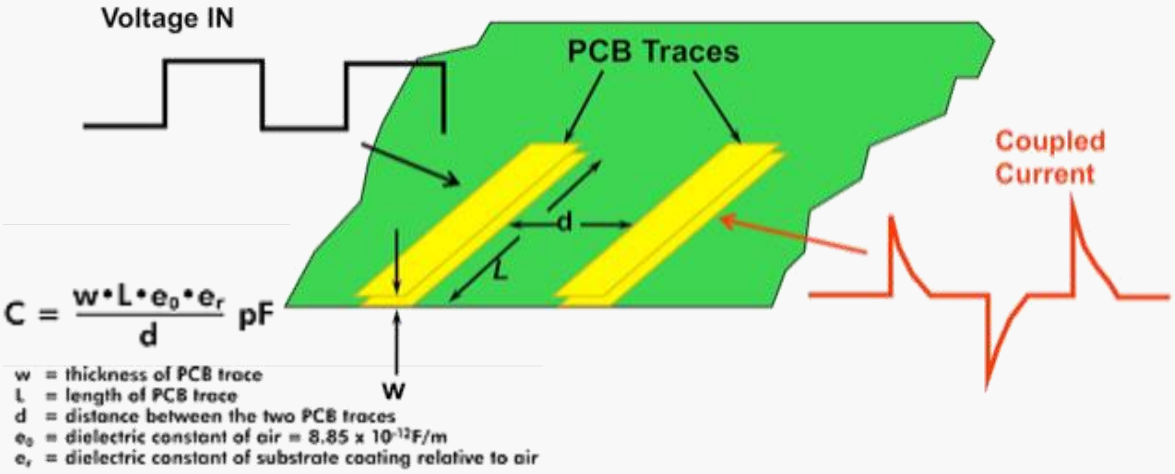

Figure 50: Illustration showing capacitive coupling effects between two PCB traces

General Routing Practices

Decoupling capacitors

A 0.1µF decoupling capacitor is placed right next to every IC power pin. The purpose of this capacitor is to shunt any high frequency noise away from the IC. This is because the power supply rejection ratio (PSSR) drops with frequency. While the PSSR graph shown in Figure 51 is for the AD8029 [20], all linear circuits and converters tend to have this general shape.

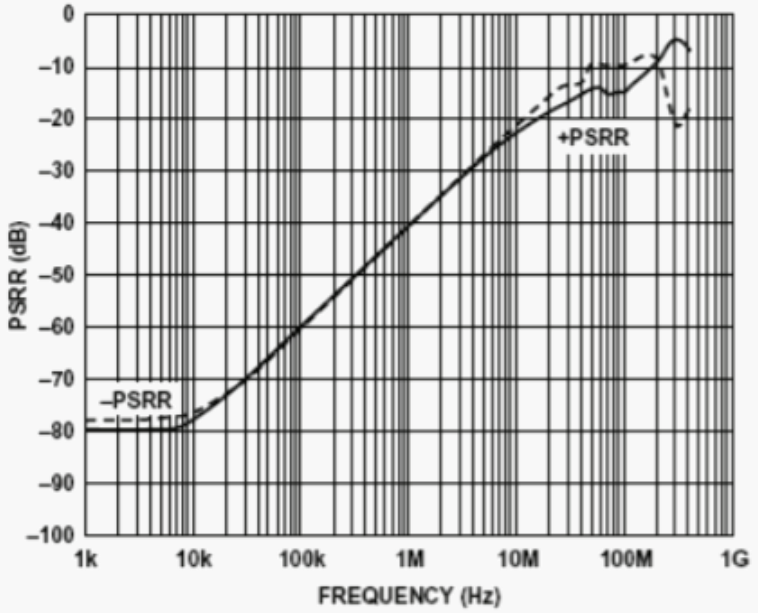

Figure 51: AD8029 PSSR Graph showing PSSR vs Frequency

Shunting the high frequency noise away from the IC helps prevent it from coupling on the output.

The capacitor needs to be place as close to the power pin as possible and needs to have a very short path to the ground plane as shown in Figure 52. This is to minimize inductance so that the capacitor can actually shunt high frequency currents. A ferrite bead can be added in series for additional decoupling if necessary. Just be sure that the added core doesn't present a new resonance problem.

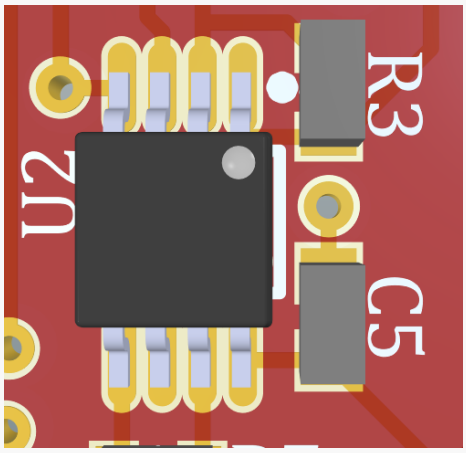

Figure 52: Decoupling capacitor placement next to IC pins

Ground and Voltage Planes

Power and grounds planes are used to lower the impedance of those nodes and help greatly in reducing ground noise. A plane offers the lowest inductance possible which is essential to minimizing potential differences in the ground/voltage plane.

Ground planes can also act as shield which can help improve the circuit's susceptibility to EMI.

Differential Signal Routing

Differential signals are two complementary signals. The advantage of differential signaling is that it is inherently immune to common mode electrical noise, the most common interference artifact found in circuits. Additionally, a common mode choke can be used to filter out this common mode. In this inverter design, there are three sets of differential PWM gate signals and the differential CAN bus signal. To ensure that the signals arrive at their destination fully complementary, the two lines should be of equal length and the impedance should be matched. The differential directive in Altium can be used for this.

Analog Signal Routing

All critical analog signals should be physically routed away from high frequency digital signals. This will prevent any noise from being capacitively coupled onto the analog lines.

3D Modeling

With this being a multi-board design, we modeled every component down to the last resistor to ensure that we didn't run into any interference issues during assembly. 3D models are also extremely useful for verifying that the footprint is correct. For standard passive components like resistors and capacitors, generic solids can be used. For unique components, the manufacturer usually provides a STP file that can be imported into Altium. 3Dcontentcentral.com is good repository for finding of 3D components if the model is not provided by the manufacturer.

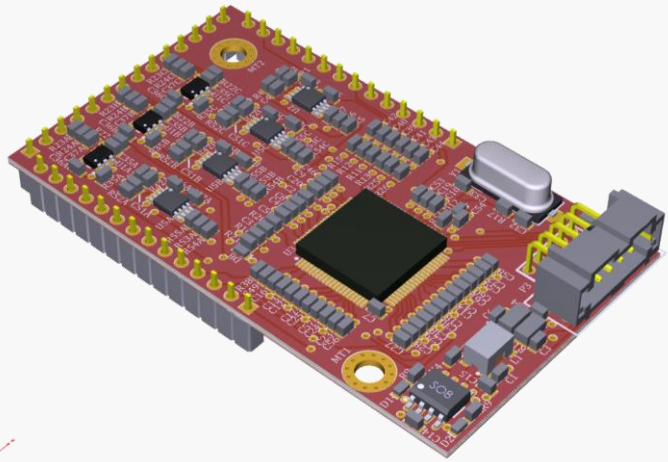

Figure 53: 3D model of control card

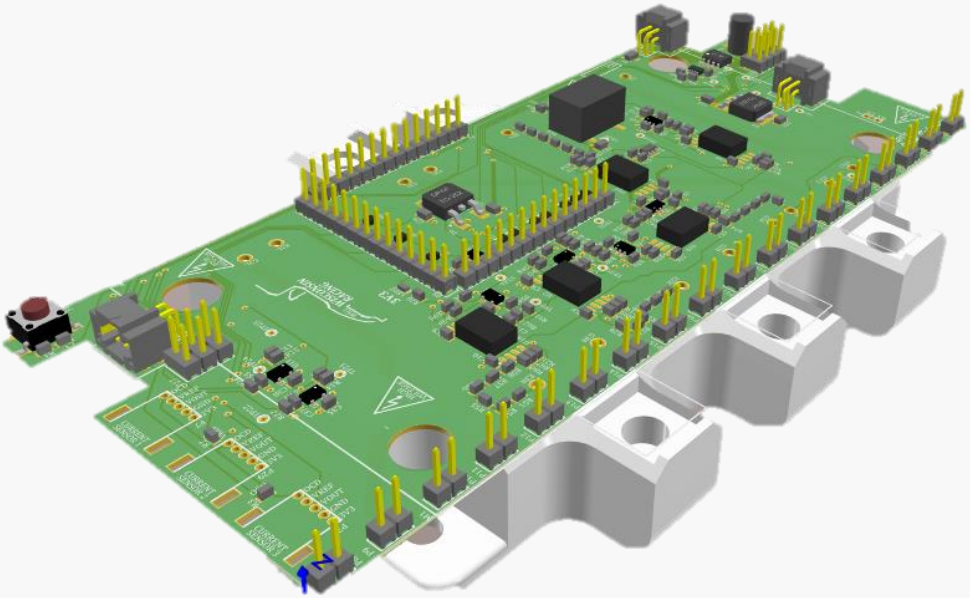

Figure 54" 3d model of parent board

Motor Controls

Control System Requirements and Goals

- Control current at switching frequency of 20kHz
    - Previous inverter: 1ms (inverter limited)
    - Hardware overcurrent protection
- Field oriented control
    - Flux weakening
    - Control torque and limit speed for chassis controls
- Increase continuous current rating to 280A
    - Previous: 180A pulse, lower due to thermals
- 1700 Hz Fundamental -> 20 kHz switching (12 per period)
    - Previous inverter: Switching also limited by low inductance of Nova motors.
- Self-sensing position control
    - Advantage in our application due to robustness / packaging vs encoder
    - Can obtain 3 electrical degree accuracy
- CANbus Communication with ECU
- High reliability and stability

Controls

TI InstaSPIN was used as the base library for the inverter firmware. It is primarily a field-oriented control (FOC) solution with a sensorless rotor position observer called FAST (flux, angle speed, and torque), and space vector modulation implementation.

A key decision in the inverter controls was in choosing to implement torque control or speed control, which was largely decided by vehicle level chassis controls. The integrated torque vectoring and traction control algorithm is based solely on the available torque at the tire, which is estimated by a friction ellipse model. Also, the motor can be very well characterized by dynamometer testing, making its torque control an order of magnitude more accurate than any tire model. Therefore, torque control is the chosen method, rather than relying on a tire model to make a motor speed request.

The inverter controls generate a current reference request based on the torque request from the vehicle controller and the rotor flux estimated from FAST. While a lookup table could be used to generate the q-axis current request, the estimated rotor flux captures the effects of rotor temperature.

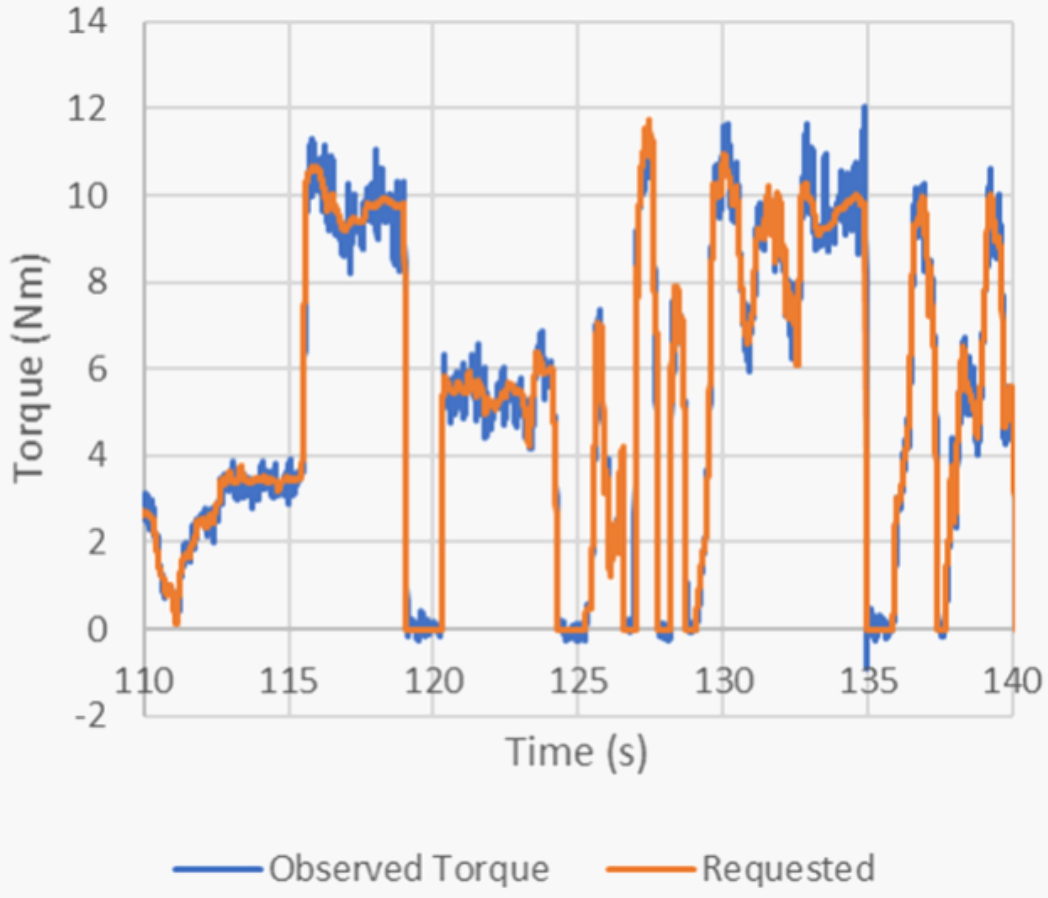

Figure 55: Torque controller testing on-vehicle with inverter estimated output torque and transient torque request.

The current regulators were set for 200 Hz bandwidth and the current reference was limited to a ramp rate of zero to full current in 1ms to minimize overshoot.

- $K_t = \Psi + (L_d - L_q)I_d$
- $I_{q,ref} = \frac{\tau_{req}}{K_t}$

State feedback decoupling based on the d-q RL motor electrical model was investigated. This improves the transient response of the current regulators, particularly for wheel lifts. However, it was found that the cross-coupling terms injected very high frequencies into the control system, causing instability in many cases. Therefore, only back-EMF decoupling was used, which largely captures the desired effect of preventing overcurrent events during wheel lifts.

$$V_{d,SFB} = r_s i_d + L_q i_q \omega_e$$

$$V_{q,SFB} = r_s i_q - (L_d i_d + K_e)\omega_e$$

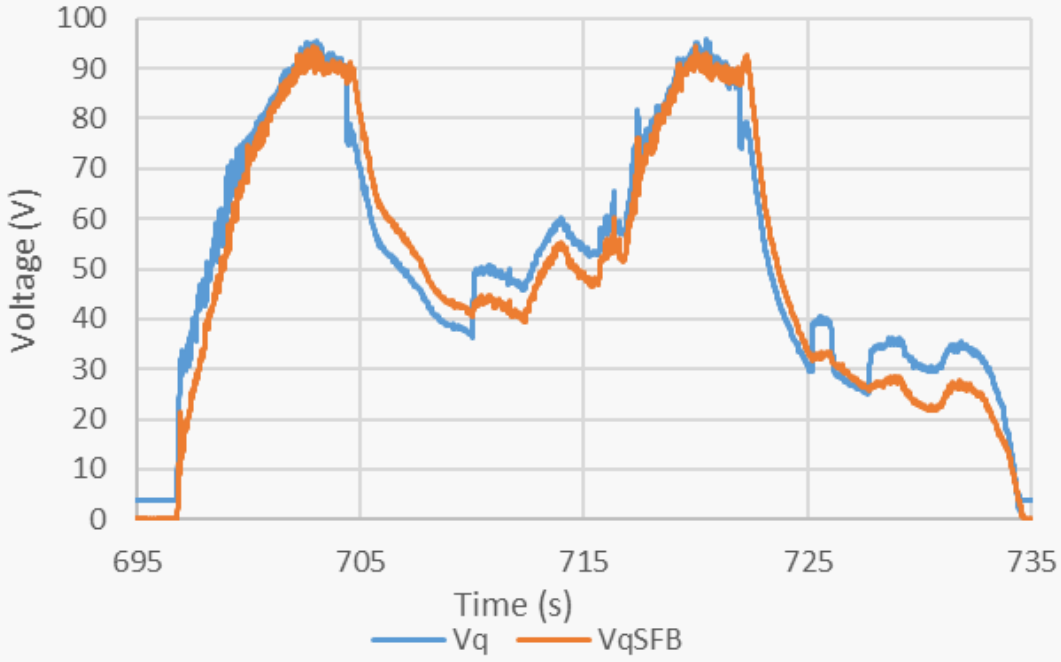

Figure 56: State feedback testing on-vehicle with only back EMF decoupling enabled.

Rotor Position Estimation

Self-sensing control of electric machines is a strategy that has been used in HVAC and other applications with low load at startup. However, it has rarely been used in traction applications. One of our key motivations in using self-sensing control is to bring the technology to the automotive sector. The position accuracy is on the order of 2° electrical angle, which is as accurate as the resolution of a 1000 PPR encoder for a 10-pole motor. The accuracy of self-sensing control increases relative to encoders for high pole pair motors, as self-sensing rotor position inherently acts on the electrical fundamental rather than the mechanical position.

Startup can be achieved several ways. The best method is using high frequency injection to determine initial position by the machine saliency. However, this requires a higher switching frequency than possible with IGBTs. The next two methods are open loop startup with transition to closed loop position observer. The first is an open loop frequency ramp that can be tuned for a given torque value based on the coupled rotational inertia and mass of the vehicle. The more robust method which was used is a fixed frequency input to generate a back EMF that can be then used to determine the d-axis location and switch to closed loop position observer.

Flux Weakening

The interior permanent magnet motor was designed with a constant power region to match the rules mandated by the 80kW battery power limit. That is, the motor reaches its constant power region at the same time the vehicle reaches the 80kW power limit during an acceleration event. To implement a constant power region in a permanent magnet machine, flux weakening control of the d-axis current is required. The reference d-axis current value was generated with a simple incremental integrating controller, which attempts to maintain the applied voltage vector as less than 90% of the DC bus voltage. This simple controller is extremely robust and handles magnet temperature variation and a non-stiff DC bus.

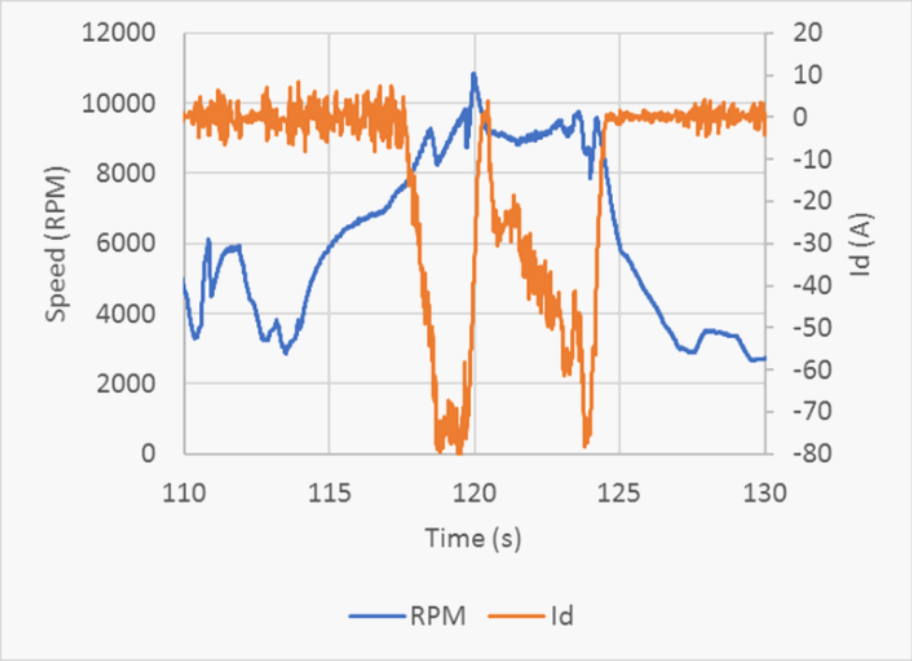

Figure 57. Flux weakening testing on vehicle – i_d begins to increment at 90% of base speed.

Fault Handling

The inverter has a hardware overcurrent protection circuit that disables all gate driver output when a high phase current threshold is reached to protect the power module. The microprocessor also monitors this fault signal and sends a CAN bus request for the main battery contactors to be opened by the BMS in the event of a hardware fault. Similarly, the gate driver features IGBT shoot-through protection via desaturation detection which is treated as an overcurrent fault by the microprocessor. Other software faults include software overcurrent protection, logic for handling bus undervoltage vs. disabled DC bus, vehicle controller CAN watchdog, implausibility in measured signals, and overtemperature protection.

Cold Plate Design

Properly cooling an inverter is the difference between high performance and thermal disaster. This section covers how I went about designing a custom cold for the inverter assembly.

Define System Targets and Constraints

The inverter needed to be water cooled to achieve the high-power density required. The cold plate designed achieves the following targets:

- Maintains steady temperature at peak heat flux under limited coolant flow rate, temperature, and pressure drop
- Interface with the IGBT thermal baseplate
- Improve heat transfer compared to a commercial cooler
- Reduce pressure drop compared to a commercial cooler
- Reduce weight compared to a commercial cooler

The plate's dimensions were limited by the stack-up of the power electronics, capacitor bank location, and the inverter case. A dual plate parallel layout was selected to achieve the most cooling area with the available real estate (Figure 58). Two inverters share a cold plate. Each plate uses a dual pass channel to return the fluid and keep coolant routing simple.

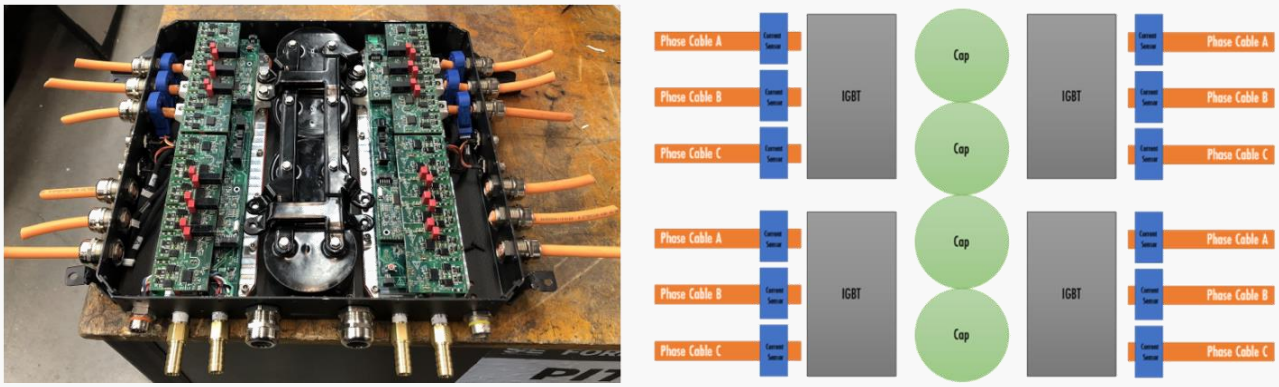

Figure 58: Quad-Inverter assemble: Two inverters share a cold plate. Each plate uses a dual pass channel to return the fluid and keep coolant routing simple

Build a Thermal Map

The first step in cold plate design is to develop a thermal map. The following information is needed and pre-determined by pump selection:

- Coolant composition: H_2O
- Flow rate: 12 [LPM]
- Inlet temperature: 35 [C]
- Available pressure drop: 10 [KPA]

I used the ε-NTU method to size and predict heat transfer performance of initial geometries. The Thermal Capacity (UA) represents heat transfer based on the convective surface area (A) and the max heat

transfer coefficient (U). U depends on fin geometry, material heat transfer coefficient, and the fluid heat transfer coefficient [21].

The following specs were found from the Infineon FS200R07PE4 IGBT and used to create a thermal resistance model.

- Junction to case resistances
  - IGBT: R_{JC} = 0.33 K/W
  - Diode: R_{JC} = 0.6 K/W
- Operating temperature limit: (T_{lim}) = 150°C
- Heat transfer equation: $q = (T_{lim} - T_{coolant})/R_{J\_Total}$

The Infineon website features a simulation tool called IPOSIM to model inverter losses. A cold plate surface temperature limit of 70°C was calculated to achieve a desired continuous IGBT current limit. That corresponds to a heat rejection requirement of 3kW across two IGBTs with a 1.2x safety factor.

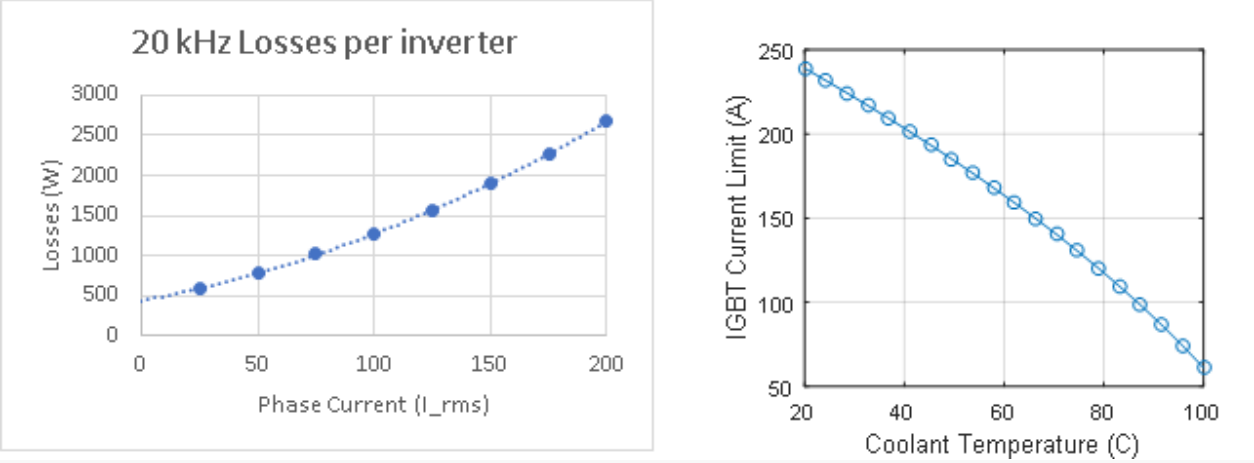

Figure 59: Single inverter loss model (left) and steady state current limit for a 150C junction temperature

Concept Development & Testing

I used Fluent CFD to predict conjugate heat transfer and pressure drop. The insight allowed me to quickly iterate through designs. The following boundary conditions were imposed to the cold-plate and fluid volume geometries:

- Mass flow water outlet
- Water inlet temperature
- Heat Flux at IGBT-Plate interface

It was important to establish a baseline and correlate the CFD and thermal models with tested data. The v1 cold plate design was a bare-bones U-channel. The simple design allowed for quick prototyping and testing. Temperature and pressure were recorded and used as a baseline to track iteration progress and to dial in the CFD model.

The cold plate design target was to achieve less than 10% of the total junction-case thermal resistance. The initial concept featured pin fins to maximize convective surface area and induce turbulent flow. Pin dimensions were calculated to maximize surface area and maintain the same hydraulic diameter through the channel as the inlet. The plate was CNC machined from billet aluminum and tested. It met heat rejection targets at 3kW but had a pressure drop of 50 kPa (target = 12 kPa).

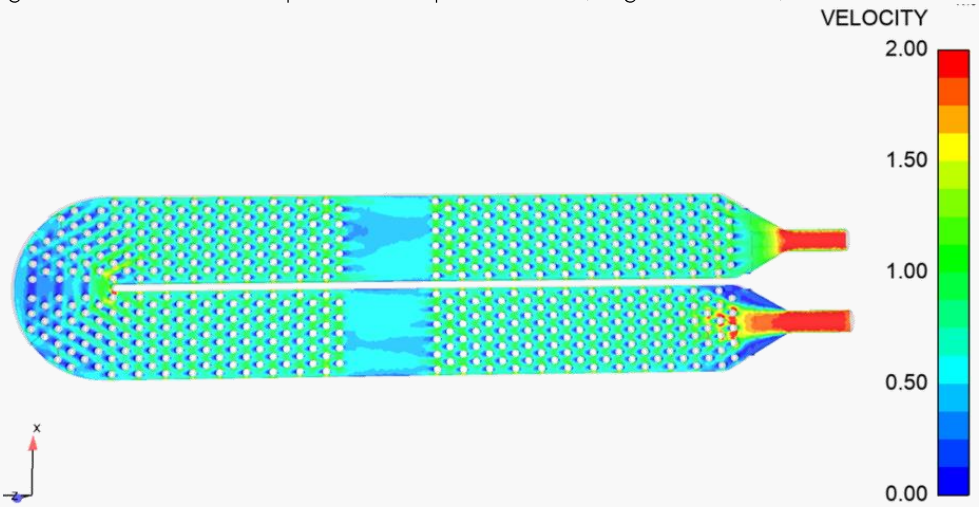

Figure 60: Pin fin design with coolant fluid volume colored by velocity and featuring velocity vectors

The cooling channel was redesigned to a wave pattern (Figure 61) allowing for higher velocity flow and eliminating the dead zones occurring behind pins (Figure 62). The waved channels also allow for more contact area between the fins and high velocity flow. Wave amplitude and frequency were optimized to disrupt establishing laminar boundary layers at the fin channel faces.

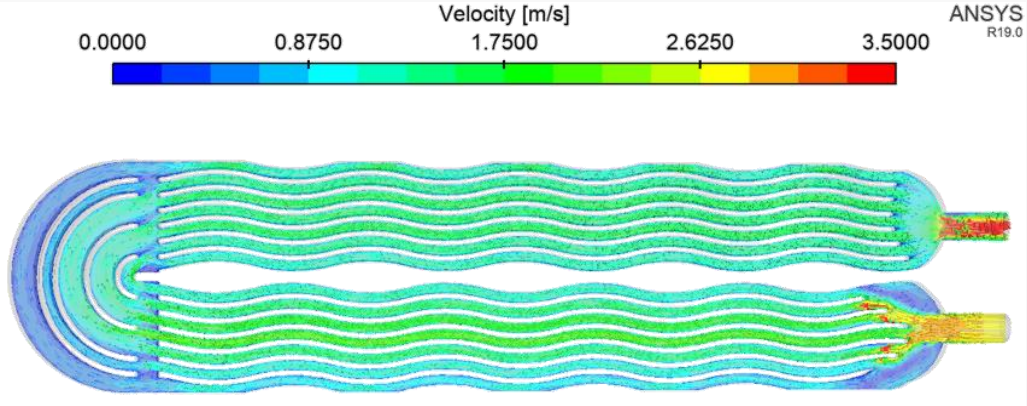

Figure 61: Waved fin design with coolant fluid volume colored by velocity and featuring velocity vectors

The CFD model was used to refine the channel geometry for the desired tradeoff between heat transfer and pressure drop. Pressure drop was further reduced by adding multiple turning vein features at the 180-degree bend. Turning veins help direct fluid flow around the bend and avoid creating stagnant dead zones. The waved design achieved 3.2 kW heat transfer rate with a 10kPa pressure drop.

Mechanical Packaging

The mechanical enclosure was designed around the power electronics, capacitor bank, and cold plate. The goals with the enclosure were to maximize packaging density, serviceability, and have excellent ingress protection. It is made out of 6061-T6 Aluminum 2mm sheet that was bent and cut by our sponsor – Engineering Metal Products (EMP). The CAD was designed in SolidWorks.

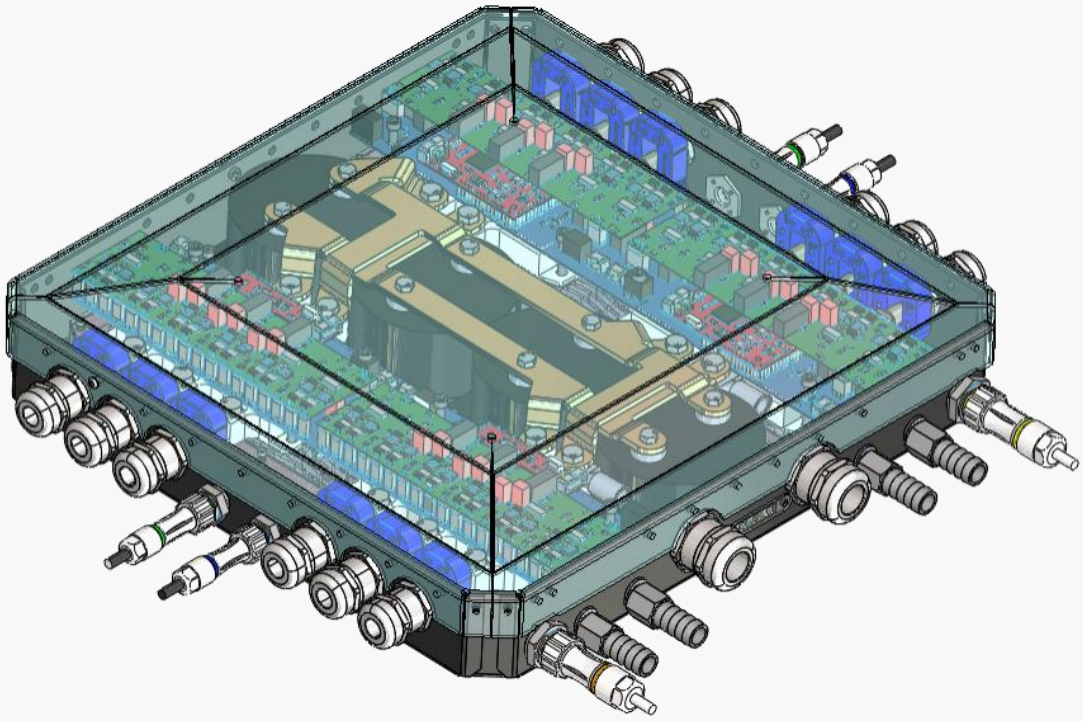

Figure 62: Isometric view showing mechanical packaging

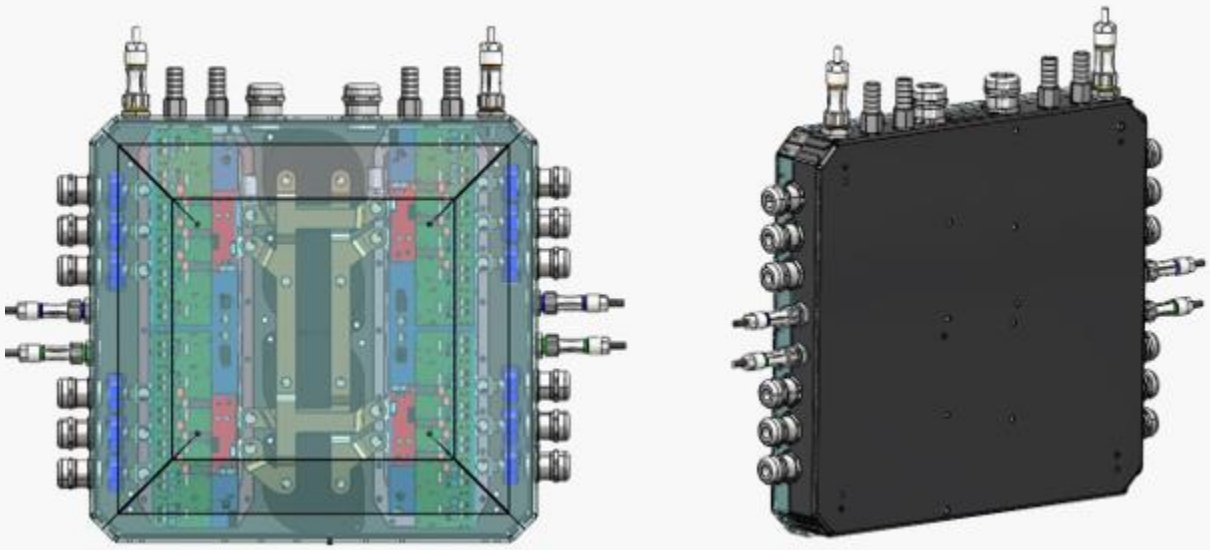

Figure 63: Alternate views of mechanical packaging

Connectors and Cables

LAPP SKINTOP cable glands were used for strain relief of the HV cables, ingress protection, and grounding of the HV cable shield.

Figure 64: Lapp SKINTOP Cable Glands

For high voltage cabling, 50mm^2 orange shielded cabling was used for the DC connections and 16mm^2 used for all phase connections. To determine cable cross section, our lap simulation tool (LapSim) was utilized to generate a current draw histogram over one autocross lap. From that, we used the thermal derating curves provided by Coroplast to determine the cross section needed to shepherd the high currents.

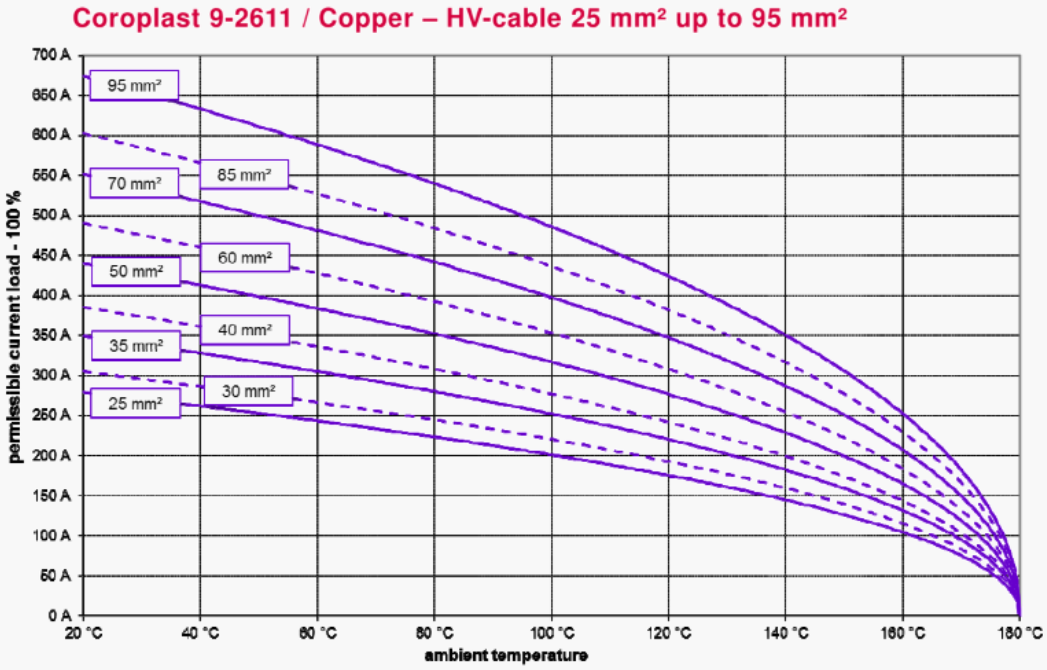

Figure 65: Derating curve for shielded silicon cable 25mm^2 - 95 mm^2

Samtec AccliMate™ IP68 Sealed connectors are used for all low voltage connectors. These are great because you can buy cable assemblies straight from Samtec. No crimping necessary - higher reliability.

Figure 66: Samtec AccliMate connectors used for all low voltage connections

To waterproof the case, a silicone gasket was bonded to the cover on the clamping surface. All connectors and cable glands came with a rubber O-ring for ingress protection. Water tests were performed to ensure the case was completely sealed.

Fabrication and Assembly

PCB Manufacturing and Assembly

All PCBS were manufactured and assembled by our sponsor – Screaming Circuits. We sent them the fabrication files and then about two weeks later, we received fully assembled boards. We are very grateful for our partnership with them.

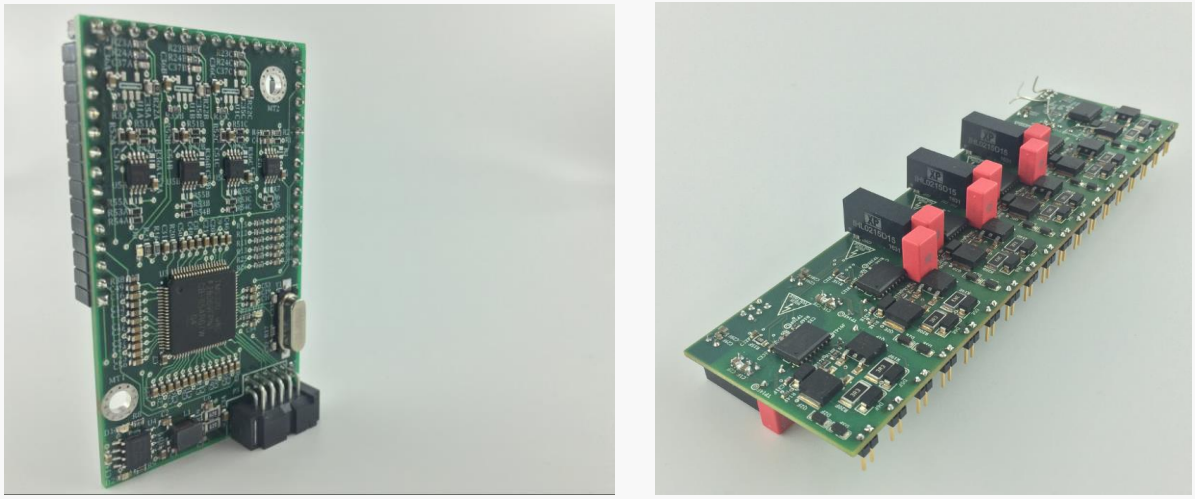

Figure 67: Manufactured v1 Control Card and Gate Driver

Case and Cold Plate Manufacturing

The case was designed to be constructed out of 2mm aluminum sheet. Our sponsor, Engineering Metal Products (EMP), laser cut and bent the sheet metal into its final shape. Once we received the case from EMP, all that was left was TIG welding the seams and painting it.

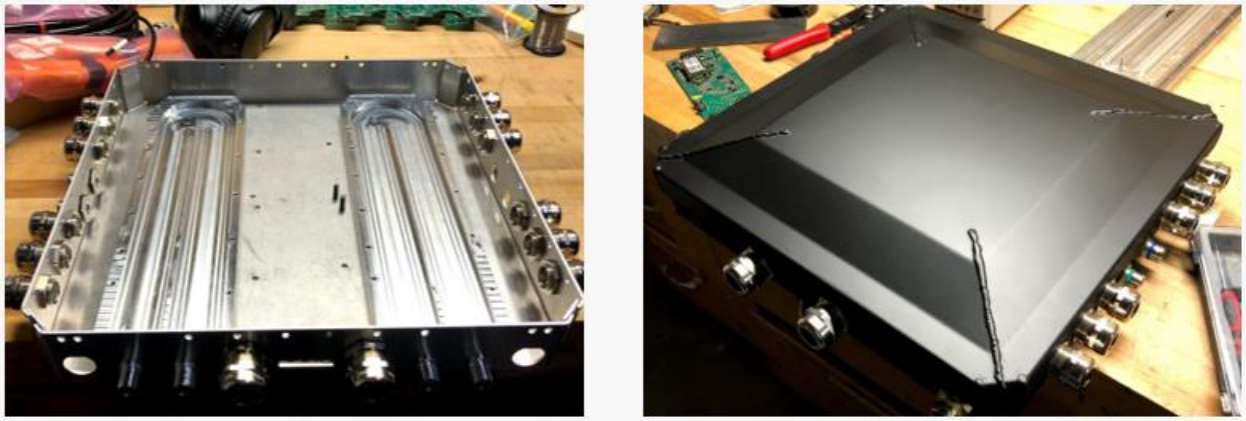

Figure 68: Inverter case with cold plates (left). Inverter cover (right)

Cold Plate Design for Manufacturing & Assembly

Before designing for fluid flow, the enclosure needs to be complete with the following mechanical design criteria:

- Packaging constraints
- Mounting - islands may interfere with fluid path
- Inlet/Outlet mapping
- Sealing
- Design for manufacturing / design for assembly
- IGBT interfacing
- Fastening/joining

The cold plate was designed as a two-part aluminum assembly. The interface between halves was sealed by a high temperature silicone gasket. The material was selected for its reliability, high temperature range, and conformability. An O-ring and groove were investigated but posed problems as the groove stole height real estate away from the fluid channel and O-ring joints designed by student engineers are prone to leak.

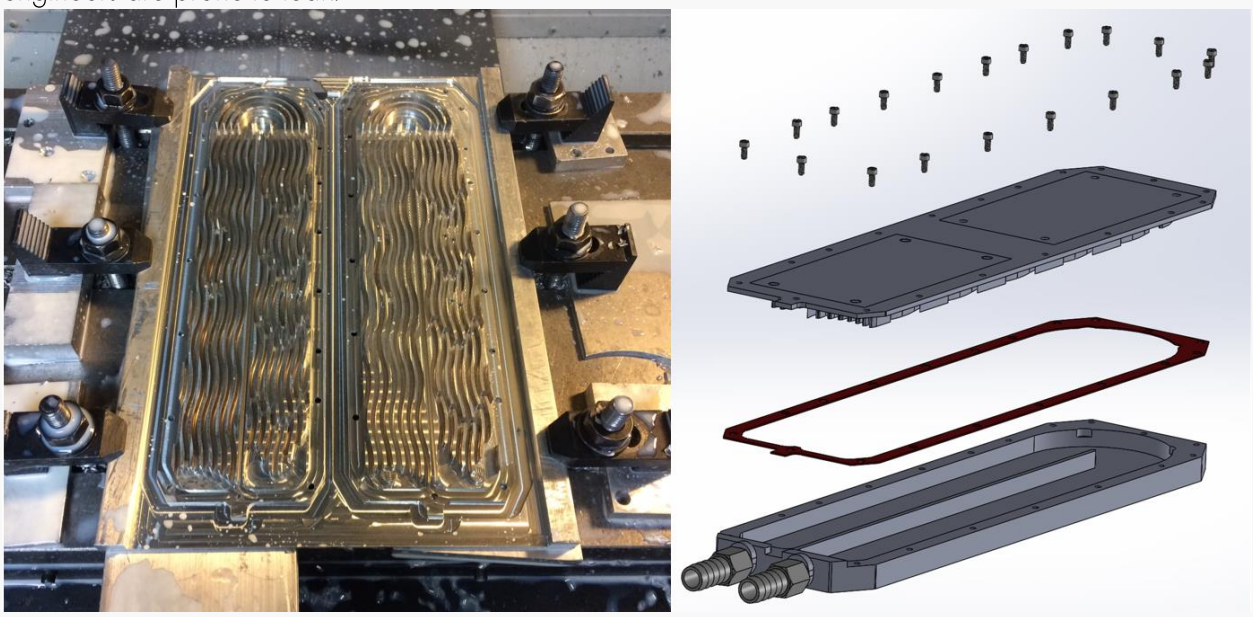

Figure 69: CNC machined fin channels (left) and exploded view of cold plate assembly (right)

The aluminum parts were designed for 3-axis CNC machining. The waved channels were enforced to be larger than the ⅛" to account for tooling. Fin height and undercuts were considered to minimize machining time and complexity. It's important to achieve a fine surface finish to reduce contact resistance between the IGBT and cold plate. The inlet and outlets were designed to incorporate standard barb NPT fittings because of their reliability and availability.

Final Assembly

Thanks to the extensive 3D modeling done with the PCBs and the power electronics, we didn't run into any significant issues when assembling. Everything fit together rather seamlessly and we were very pleased with the packaging as there was very little unutilized space. The final quad inverter assembly is shown in the image below.

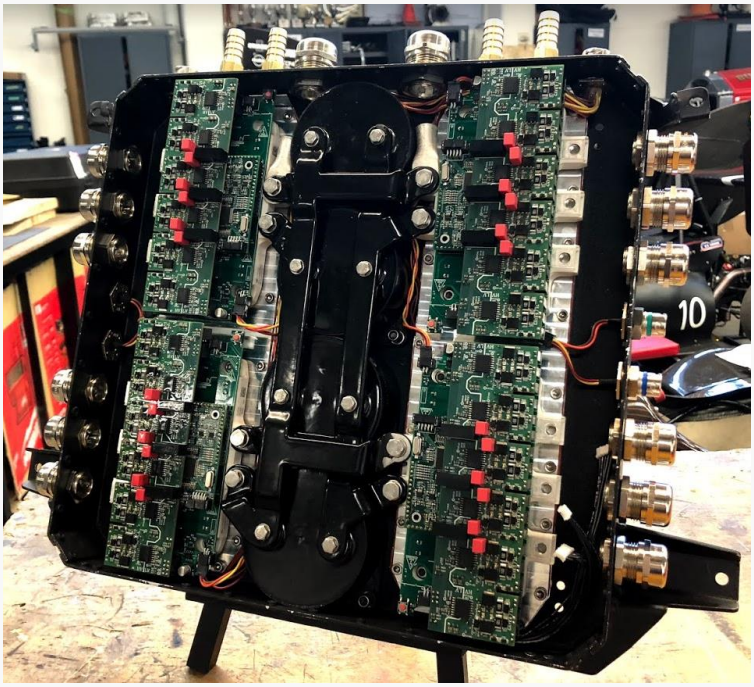

Figure 70: Final Quad Inverter Assembly (current sensors not shown)

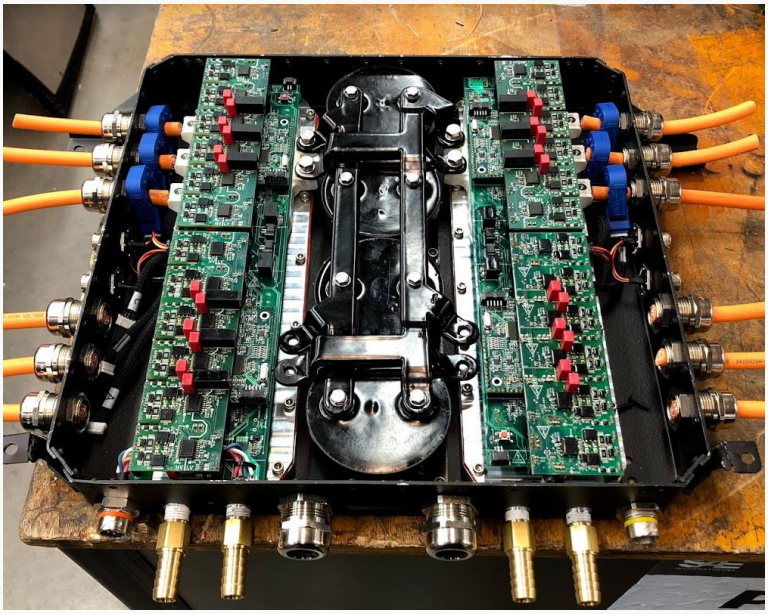

Figure 71: Final Quad Inverter Assembly view 2

Weight Stackup

We tried to optimize the design for the inverter to be as light as possible. The table below shows the weight stackup for the quad inverter. The AMK quad inverter package (off-the-shelf alternative) weighs 11.5kg [24], making it 2.6kg heavier than ours. Not bad!

Item	Weight (grams)	Qty	Total Weight (grams)	Estimated from CAD?
DC link caps	316	4	1264	
DC Cable Glands	60	2	120	
Phase Cable Glands	40	12	480	
PCB Assembly	232	2	464	
IGBT	300	4	1200	
Current Sensor	32	12	384	
Case	1000	1	1000	Yes
Cover	1000	1	1000	Yes
Cold Plate	900	2	1800	Yes
Busbars	75	2	150	Yes
12V LV connectors	30	5	150	
16mm LV connector	52	1	52	
Fasteners	100	1	100	
Total Weight			8164	
Actual Weight			8.9kg	
Hypothesis is that 0.8 kg delta is due to the weight of the cold plates being higher than expected				

Figure 72: Weight stackup of quad inverter

Testing

The inverter was rigorously tested before being used on the vehicle. The firmware was first validated with a development kit from TI, with only small modifications being made for the prototype inverter (such as CAN bus communication). After bench testing the prototype the inverter with a low voltage DC bus, the inverter was tested on a dynamometer with a high voltage DC bus.

Design Validation Plans and Reports (DVP&R)

For each board, we created a design validation plan & report (DVP&R) to document all testing for hardware functionality and to ensure it met initial requirements. In the DVP&R, each test is given a name, description (how will the test be performed), acceptance criteria, and the prerequisite equipment needed to perform the test. Everything is documented in this spreadsheet- from a simple smoke test to validating the frequency response of a filter.

Design Verification Plan & Report

Purpose: Validate the functionality of hardware on the Quad Inverter parent board with control card and gate driver connected	**Formula SAE Electric**
	PART NAME: Quad Inverter Parent Board
	Testers: Jason Sylvestre
	Test Date: 1/4/2018 - 1/30/2018

TEST PLAN

Test Name	Test Description	Acceptance Criteria	Prerequisites	Results
Smoke Test LV	Connect 12V and GND to header pins	No magic smoke, 3V3 blue LED and 5V blue LED illum.	Power supply	PASS
Smoke Test HV	Connect 5V to HV+ and HV-	No magic smoke	Power supply	PASS
5V	Measure 5V on TP5. Capture waveform	± 1%, blue LED	Power supply, Oscope	PASS
3V3	Measure 3V3 on TP7. Capture waveform	± 1%, blue LED	Power supply, Oscope	PASS
3V3REF	Measure 3V3REF on TP4. Capture waveform	± 0.05%	Power supply, Oscope	PASS
1V65REF	Measure 1V65REF on TP1. Capture waveform.	± 0.05%	Power supply, Oscope	PASS
ISO_5V	Measure ISO_5V on TP6. Capture waveform.	1.20%	Power supply, Oscope	PASS
ISO_3V	Measure ISO_3V3REF on TP3. Capture waveform. Remember measure w.r.t. to HV-	± 0.05%	Power supply, Oscope	PASS
ISO_1V65REF	Measure ISO_1V65REF on TP2. Capture waveform. Remember measure w.r.t. to HV-	± 0.05%	Power supply, Oscope	PASS
15V+,-15V	Measure 15V, -15V on gate driver when 13.5V applied	±5%	Power supply, Oscope	PASS
CAN	Connect to CAN inputs on parent board and communicate with TM4C	Successful com	VN1610, Power supply	PASS
RESET	Hit S1 global DSP reset button and observe program behavior on TM4C	All DSPs reset operation	Power supply, firmware	PASS*
Current Sensor	Measure on control card 1.65V when 0A applied. Measure on control card 3V when 3V applied to current sensor analog VOUT node	1%	Power supply, Oscope	PASS*
Phase Voltage	Measure on control card 0V when 0V applied. Measure on control card x V when 50V applied	1%	Power supply, Oscope	PASS

Sheet1 | Phase Voltage | Disable Logic | IGBT Temp | Test Logs

Figure 73: Parent Board DVP&R

Dynamometer Testing

After completing the DVP&R's for each board, we moved from component-level testing on the bench to system-level testing on a dynamometer. The Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) was gracious enough to let us use their 170kW dyne capable of four quadrant operation with a fully regenerative DC bus.

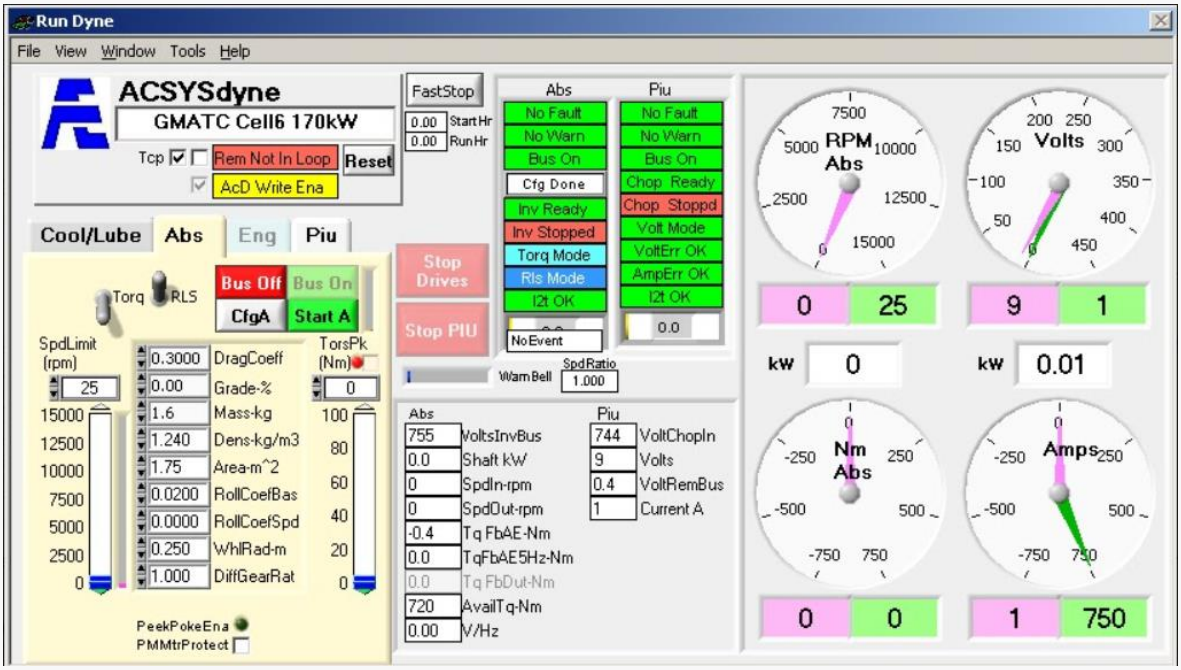

Figure 74: Dyne control interface

Current control was validated through the required frequency range of the motors. Additionally, a steady-state load of 280A was achieved for a measured IGBT temperature of 110°C, therefore meeting the goal set for continuous operation.

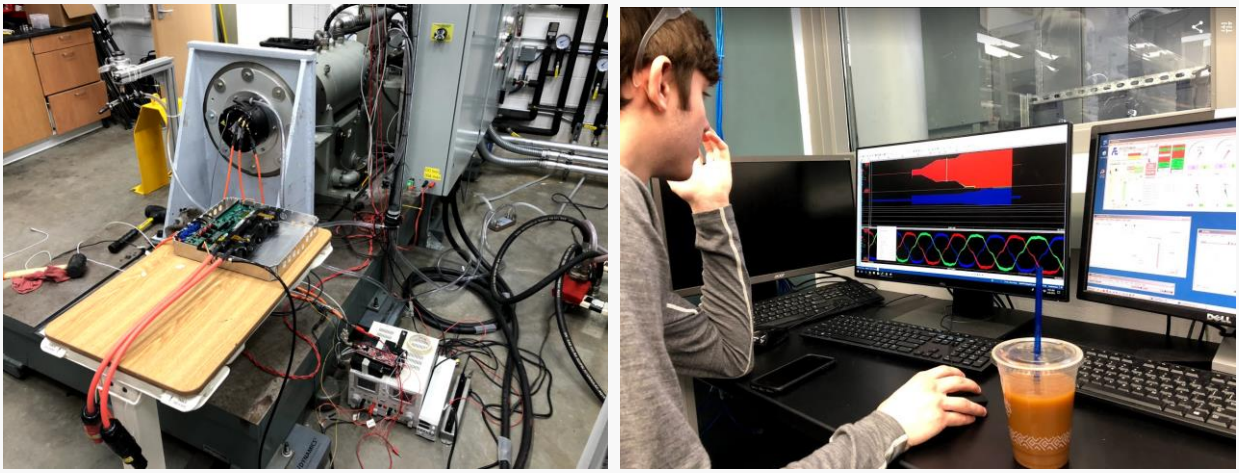

Figure 75. Dynamometer testing at WEMPEC

Vehicle Testing

The driver's safety is of the highest importance. Rigorous testing was done to ensure all inverter safety features were 100% functional in a number of different operating conditions. The first in-vehicle test was done on stands without wheels. After working through some bugs with the vehicle on stands, the vehicle was brought out to the track where we did dynamic testing. Obviously the oscilloscope could not be used for data collection so a Vector CAN bus datalogger was used to log all inverter CAN messages.

Figure 76: Vehicle testing

Discussion

I want to highlight a few key takeaways that we learned from testing.

Gate-Emitter Loop Inductance

There is no such thing as a perfect conductor. Every trace has resistance, inductance, and some capacitive coupling associated with it. The inductance can become significant when you start switching large currents at high frequencies. This phenomenon was not initially accounted for when determining the board architecture. The gate driver was chosen to live on a daughter board without much consideration given to the loop length and the resulting inductance because of it. During initial testing, we noticed large voltage overshoot on the gate signals.

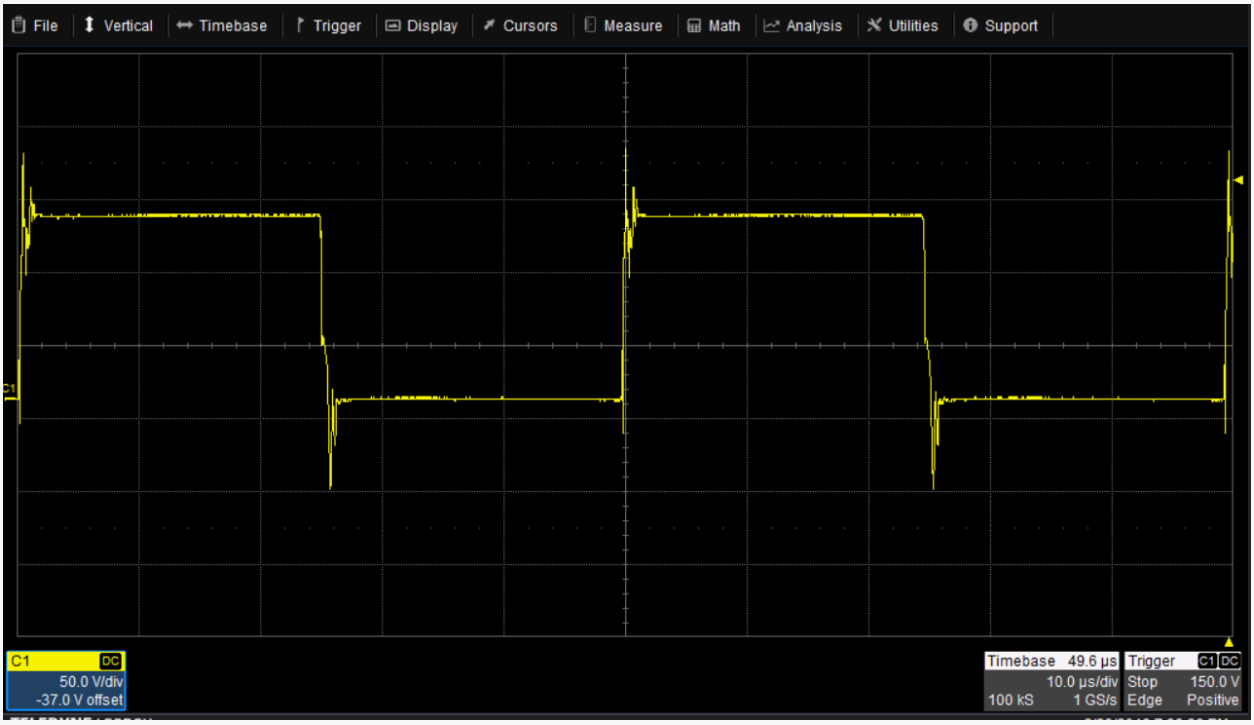

Figure 77: Ringing on gate

This ringing may have been the source of IGBT failure and introduced a number of different noise problems. This problem was solved by increasing the gate resistance by a factor of 4 to dampen the oscillations, but this band-aid fix came with negative consequences - increased switching losses and longer deadtime. In the next iteration, we will be placing the gate driver circuitry very close to the gate pins and moving the voltage sense and power supply to a daughterboard. This will address the root cause of the problem and we should be able to lower the gate resistance and reduce switching losses.

Clamp Protection

Overvoltage on an IGBT is one of the most common failure modes. When a power device turns off rapidly, the energy stored in any stray inductance is dissipated and there is voltage overshoot because of this. We saw this occur both on the gate-emitter as well as the collector-emitter. When the gate driver board was not connected and a DC bus was applied to the half bridge, there was an unclamped gate scenario. The IGBTs turned on through capacitive coupling and a shoot-through event occurred, which exploded our IGBTs. To solve this, pulldown resistors connected right between the gate and emitter pins were used to ensure that the IGBT was clamped to the off-state. Fast-acting zener diode clamps were used as insurance to protect against voltage overshoot. These two devices were added after the first round of dyno testing.

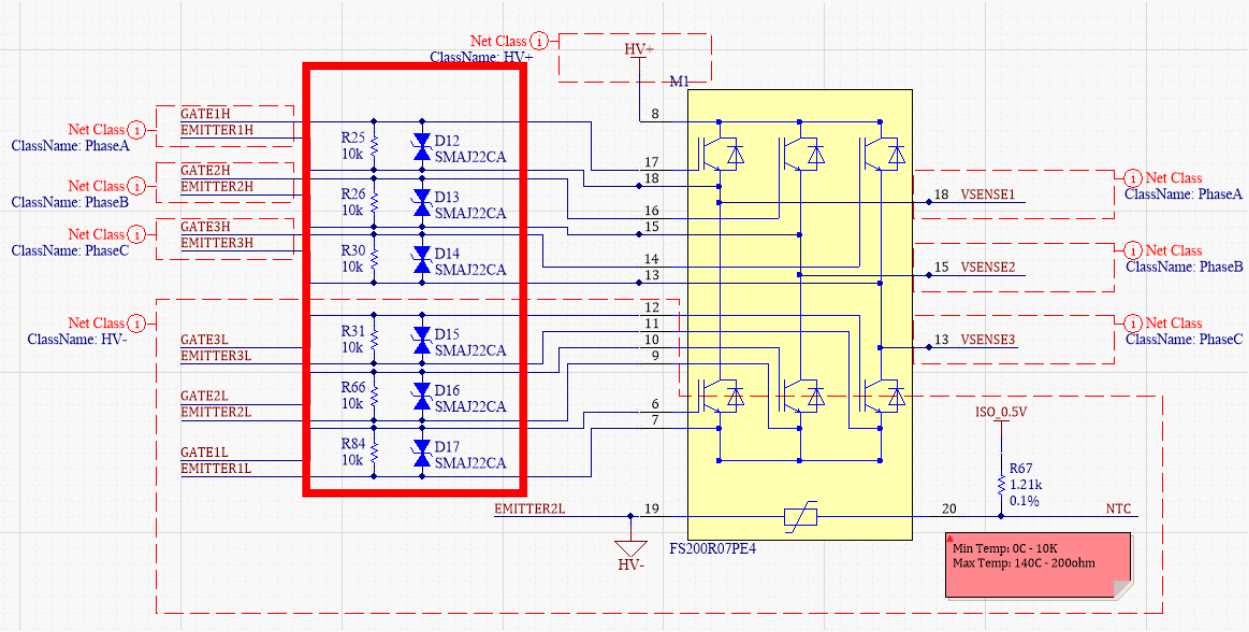

Figure 78: Zener clamp diodes and pulldown resistors

Wide Bandgap (WBG) Devices?

If we wanted to achieve faster switching frequencies, we'd have to switch to using SiC MOSFETS or GaNfets. We did a test where we pushed the switching frequency as high as we could go. With IGBTs, we lost control at any frequency above 20kHz. With WBG devices, we could switch at much higher speeds. The advantage is that the motor losses are shifted from the motor to the inverter. This could be overall beneficial as the inverter is currently overcooled even with the increased gate resistance. However, if switching frequency was increased, we'd run into CPU loading issues and would have to switch to a higher performing MCU. Unfortunately, a faster MCU equipped with InstaSPIN does not exist. With that said, we can't justify using SiC or GaN devices instead of IGBTs.

Conclusion

The off-the-shelf inverters purchased for the WR-217e were unreliable and could not continuously run at the current spec'd because of their passive cooling. As a result, they were the main components limiting the performance of the vehicle. Thus, the success of the WR-218e car very much depended on the success of the inverter project.

With that said, we are very happy with how the quad inverter turned out. Based on the extensive testing done on the dynamometer and in the vehicle, the quad inverter met all initial requirements and solved all problems posed by the WR-217e inverters.

- The car was not thermally limited this year! The liquid cold plate had no problem keeping the IGBTs within their safe operating area. We never saw IGBT die temperature rise above 70C during vehicle testing.
- Implemented Field Oriented Control, Space Vector Modulation, and sensorless rotor position estimation using InstaSPIN. By switching from from 6-step to SVM, phase current is now sinusoidal (as seen in Figure 79), which significantly reduces motor losses.

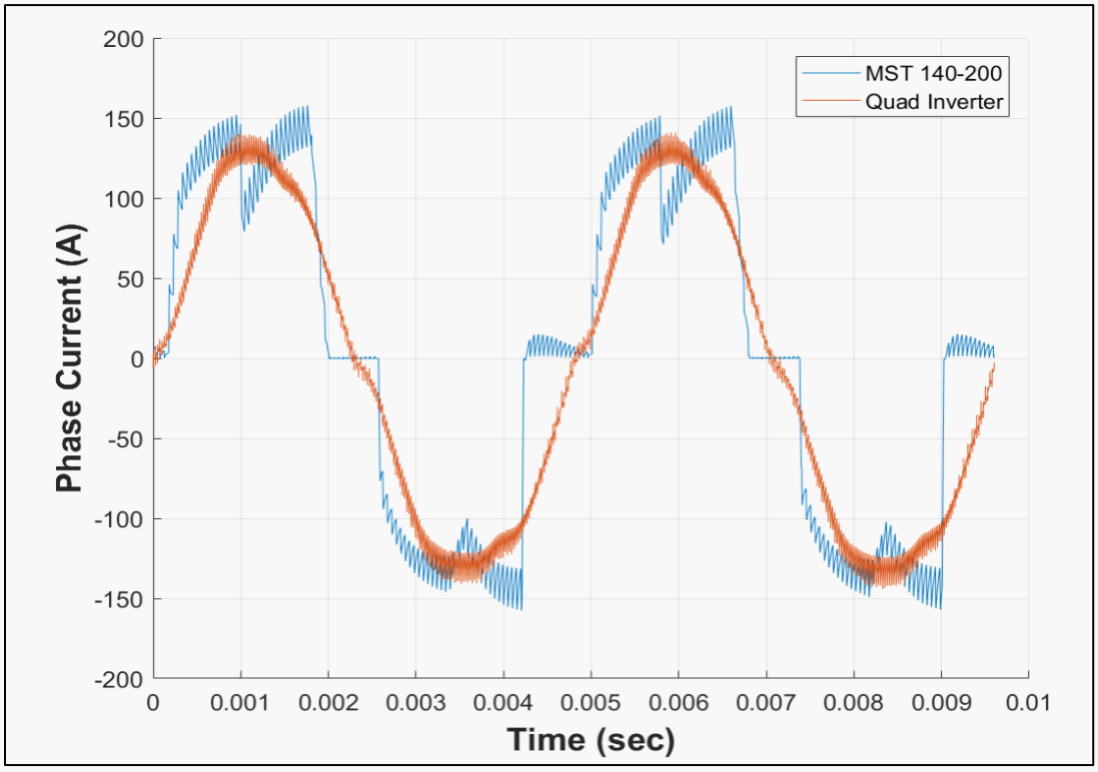

Figure 79: Phase current from the 217e inverter (MST 140-200) with phase current from the 218e quad inverter overlaid

- Safety circuitry acted many times to save our inverter and not once did we have an explosive failure during normal operation.

- FOC allowed us to implement regenerative breaking which was not possible the WR-217e inverters.
- The quad inverter fit seamlessly into our monocoque and frame. Having four inverters in one box drastically simplified high voltage wiring. Instead of 8 DC cables/connectors, there were only two. Reducing complexity is always good. The mechanical design was sound, and our waterproofing solution worked flawlessly.
- Inverter internals are accessible without needing to remove inverter from the car. This may not seem significant but was absolutely necessary in order to debug system integration problems.
- The final weight of the quad inverter was 8.9kg, making it 2.6kg lighter than the alternative AMK inverter.
- 20kHz switching frequency was achieved allowing for control of motors with a high fundamental frequency

In conclusion, the custom quad inverter met all initial requirements and outperformed off-the-shelf alternatives in terms of its power density, interfacing, safety features, and accessibility.

About the Authors

Jason Sylvestre

Jason was the leader for the inverter project. He designed all the electronics and was responsible for overall systems integration. He recently acquired a bachelor's degree in Electrical Engineering and will be pursuing a master's at the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) where he will be working on power electronics development for bearingless motor drives. After graduate school, he plans to work for a startup and then start a business of his own in the area of electrified transportation.

Will Sixel

Will Sixel was responsible for motor controls and firmware on this project. Will has a bachelor's degree in Engineering Mechanics and Astronautics and is now working towards a master's degree in mechanical engineering with WEMPEC. This fall, Will is taking his versatile skillset to work at NASA where he will be doing thermals for their High Efficiency Megawatt Motor (HEMM) project.

Alex Shozda

Alex Shozda took charge on engineering the cold plates used for cooling the power electronics. He is working on finishing up his undergraduate degree in mechanical engineering and is planning on pursuing an MBA upon graduation. His ultimate goal is to start a company as well. This past summer, Alex worked at Tesla where he helped further develop their solar roof products.

Acknowledgements

We have many people to thank for helping make this project a reality.

Thank you WEMPEC for letting us use your dyne facility to test the functionality of our inverter. This was absolutely critical to development. Additionally, thank you for the design feedback and general advice on how to tackle a custom electric powertrain.

Thank you Lenze for the monetary donation and the extensive design feedback. It was very nice to have a resource with a proven track record in motor drives that we could ask questions to.

Thank you Screaming Circuits for manufacturing and assembling all our PCBs! Your service saved us loads of time assembling and debugging manufacturing problems.

Thank you Wiha for your generous donation of electrical tools and the social media content during competition! We loved getting to know Wade and Andrew this past season and are excited to continue our partnership for many years to come.

Thank you Teledyne Lecroy for loaning us a WaveSurfer oscilloscope and probes! The scope was an absolute joy to use.

Thank you LEM for donating current sensors and providing us with design support!

Thank you Altium for allowing for the PCB design software licenses. I love using your software and will be using it for the rest of my life.

Thank you Solidworks for donating licenses to every member on the team. I've used many different modeling software and Solidworks is by far the most intuitive and enjoyable to use.

Thank you Samtec for donating all connectors and wire harness assemblies! This saved us many hours and greatly improved the reliability of our system.

Thank you Electronic Concepts for donating the DC link film capacitors. It was a pleasure working with you guys.

Thank you EMS Industrial for silver plating our busbars. This process is very important for conductivity and reducing oxidation.

Additionally, we would like to thank our advisor, Dr. Glenn Bower, for his support and guidance on the project. Last, we would like to thank the rest of the team. This project could not have been realized without all these amazing people.

Figure 80: Wisconsin Racing 2018 squad

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